



CHAPTER 5 - NOTES ON THE USE OF
SEMICONDUCTOR DEVICES

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5.1 Evaluation and Assurance of Soldering Heat Resistance

Surface Mount Devices (SMD) have become widely used in recent years due to their advantages for high density mounting. However, SMD package cracking caused by thermal stress during mounting has also become a problem.

To prevent this problem, the Sony Semiconductor Network Company improves package materials and structures, and also ranks each product according to the actual package cracking resistance (Surface Mount Device rank) in order to assure the mounting conditions to customers.

This section describes the package cracking mechanism, package moisture absorption characteristics, mounting rank evaluation and assurance contents, and cracking models.

5.1.1 Package Cracking Mechanism

5.1.1.1 Package Cracking Mechanism

As shown in Fig. 5-1, IC package cracking occurs when the package absorbs moisture, the heat during solder mounting causes moisture reaching the boundary between the chip or die pad and the molded resin to gasify and expand, and stress concentrating on the edge of the chip or die pad exceeds the resin strength.

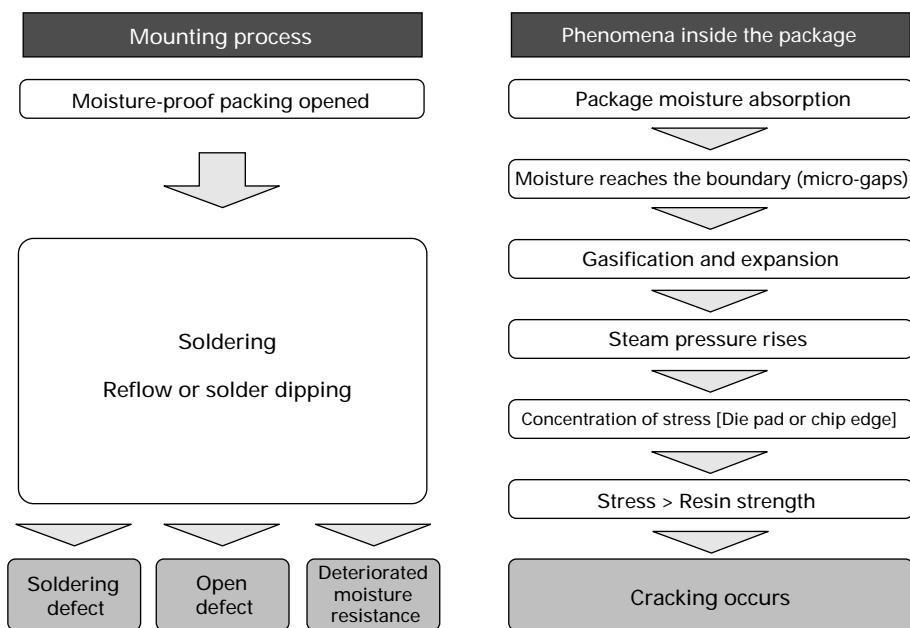


Fig. 5-1 Package Cracking Mechanism and Trouble Contents

5.1.1.2 Factors Causing Package Cracking

Package cracking generally occurs when delamination occurred between the chip or die pad and the resin, and the maximum stress σ produced by the vapor pressure P inside this gap and concentrated on the midpoint of the long edge exceeds the bending strength η (T) of the resin. The uniform load model for rectangular boards with fixed edges is applied as the analysis model at this time, and the cracking conditions are expressed by Equation 5-1.

$$\eta (T) \leq \sigma = 6k \left(\frac{a}{h} \right)^2 P \quad 5-1$$

- Where,
 a: Chip or die pad short edge length
 b: Chip or die pad long edge length
 h: Resin thickness
 k: Shape coefficient determined by b/a

Table 5-1 shows the structural, material and mounting factors corresponding to Equation 5-1.

For example, as the chip or die pad size increases, the stress increases proportionally to this square. In addition, the stress is also increased by increases in the amount of moisture absorption due to the storage environment and time after opening the moisture-proof packing.

Various methods are employed to improve package cracking resistance, such as making slits in the die pad of the lead frame, increasing the adhesive force, and using resin with low moisture absorption.

Table 5-1 Factors Causing Package Cracking

Structure	Die pad or chip size Resin thickness under the die pad or over the chip Slits	k, a h Adhesive force, dispersion of maximum stress (σ)
Materials (mold resin)	Strength (bending strength, fracture toughness value) Adhesive force Moisture absorption characteristics	$< \sigma \Rightarrow$ Cracking P
Mounting	Storage atmosphere and time Soldering temperature	P P, strength, adhesive force

5.1.2 Moisture Absorption Characteristics

5.1.2.1 Package Moisture Absorption Mechanism

Fig. 5-2 shows the package moisture absorption image and model.

Fig. 5-2 shows the images during the course of moisture absorption. After water vapor in the air is adsorbed to the resin (Henry's Law), this moisture diffuses to the inside of the package (Fick's Law) until the moisture density inside the package reaches the saturated state.^{1) 2) 3)}

Fick's Law which is applied as this diffusion model is obtained as Equation 5-2 by giving the initial and boundary conditions shown below and solving.

The moisture density at the boundary between the chip or die pad and the resin can be obtained using Equation 5-2.

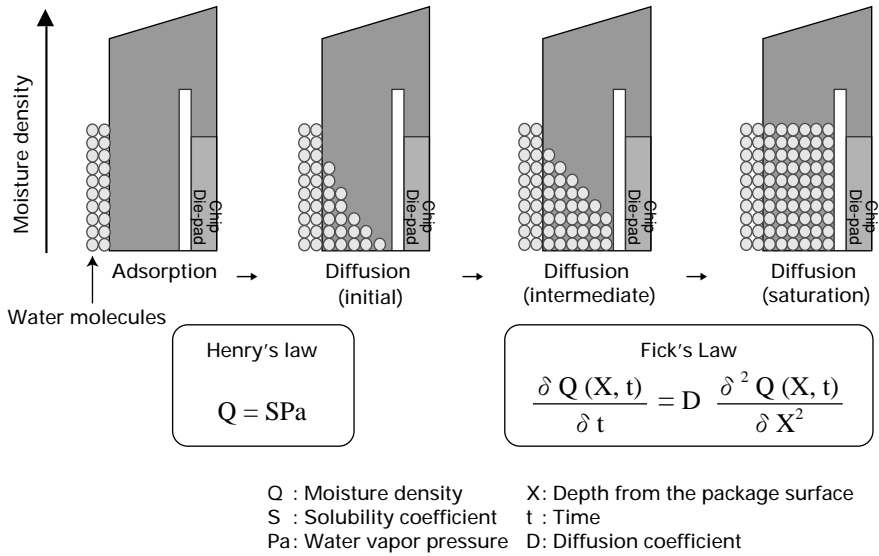
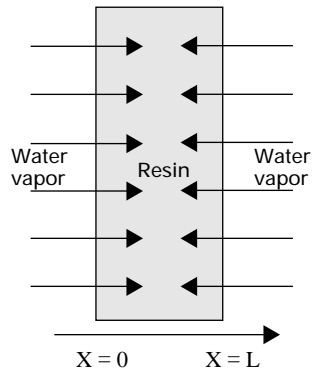


Fig. 5-2 Package Moisture Absorption Model

Initial conditions: $Q = Q_0 (0 \leq X \leq L, t = 0)$

Boundary conditions: $Q = Q_s (X = 0, L, t > 0)$
 $= SPa$
 $= SO \exp(E_s/k \cdot T) \times Pa$

Q₀: Initial moisture density E_s: Activation energy
 Q_s: Saturation moisture density k : Boltzmann's constant
 S: Constant T : Absolute temperature



Note) X=L/2; resin thickness under the die pad or over the chip

Moisture density

$$Q(X, t) = Q_0 + (Q_s - Q_0) \left\{ 1 - \frac{4}{\pi} \sum_{n=0}^{\infty} \frac{1}{(2n+1)} \sin\left(\frac{(2n+1)\pi}{L} X\right) \exp\left(-\frac{(2n+1)^2 \pi^2}{L^2} Dt\right) \right\}$$

5-2

$$D = D_0 \exp\left(\frac{E_d}{k \cdot T}\right)$$

D : Diffusion coefficient k: Boltzmann's constant
 D₀: Constant T: Absolute temperature
 E_d: Activation energy

Note) The activation energy symbol is normally E_a.
 When obtaining the solubility coefficient: defined as E_s
 When obtaining the diffusion coefficient : defined as E_d

5.1.2.2 Verification of Moisture Density (Theoretical Value)

It is impossible to directly measure the moisture density inside a package. Therefore, the theoretical value obtained from Equation 5-2 is verified using the moisture absorption amount (rate) as shown below.

The package moisture absorption amount $M(t)$ is obtained by integrating the moisture density shown in Equation 5-2 by X for $[0,L]$,

$$M(t) = L \left\{ Q_0 + (Q_s - Q_0) \left(1 - \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{1}{(2n+1)^2} \exp \left(-\frac{(2n+1)^2 \pi^2}{L^2} Dt \right) \right) \right\} \quad 5-3$$

Note that Equation 5-3 shows the amount of moisture absorbed per unit area.

Fig. 5-3 shows an example comparing theoretical moisture absorption rate values obtained using Equation 5-3 with actually measured values. The theoretical and actual values match closely, indicating that the moisture density obtained from Equation 5-2 can be accurately applied to the package moisture absorption amount.

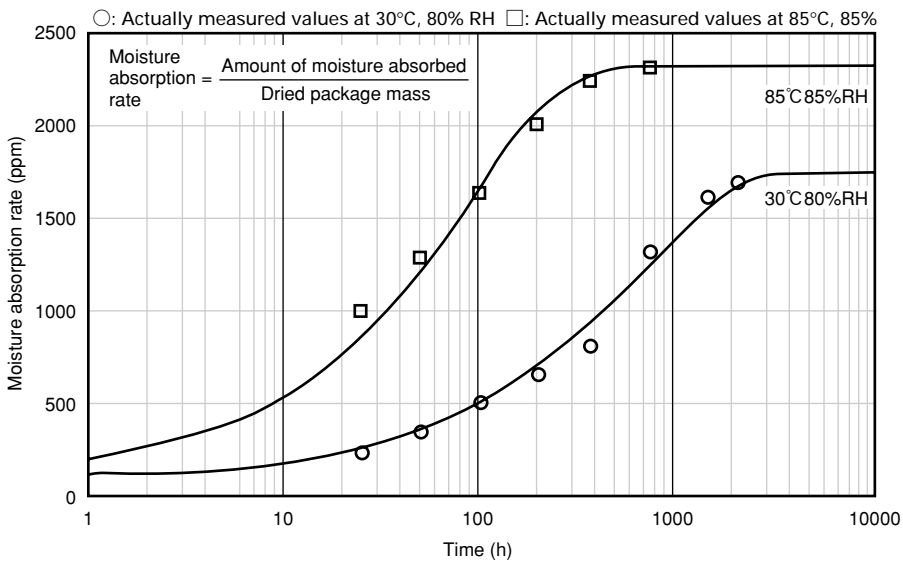


Fig. 5-3 Comparison of Theoretical Package Moisture Absorption Rate Curves with Actually Measured values for an 80-pin QFP

5.1.2.3 Package Moisture Absorption Simulations

Package cracking is determined by the moisture density at the boundary between the chip or die pad and the mold resin shown in Fig. 5-4.

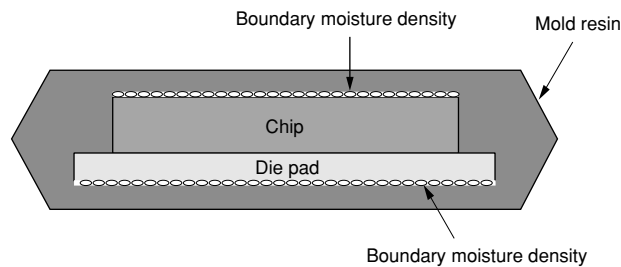


Fig. 5-4 Boundary Moisture Density Image Drawing

This boundary moisture density is obtained through simulations using equation 5-2.

Fig. 5-5 and Fig. 5-6 show simulated boundary moisture density curves for a QFP package with relatively thick resin and a TSOP package with relatively thin resin.

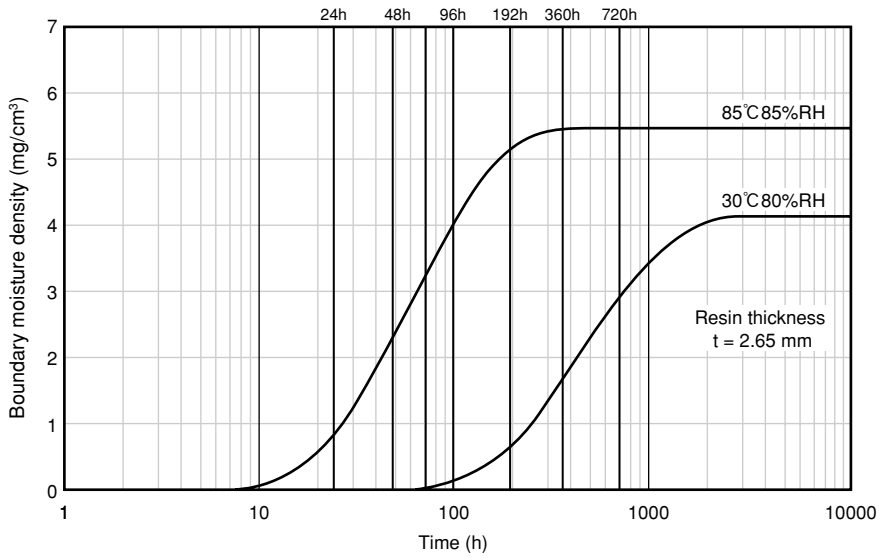


Fig. 5-5 Simulated Boundary Moisture Density Curves for an 80-pin QFP

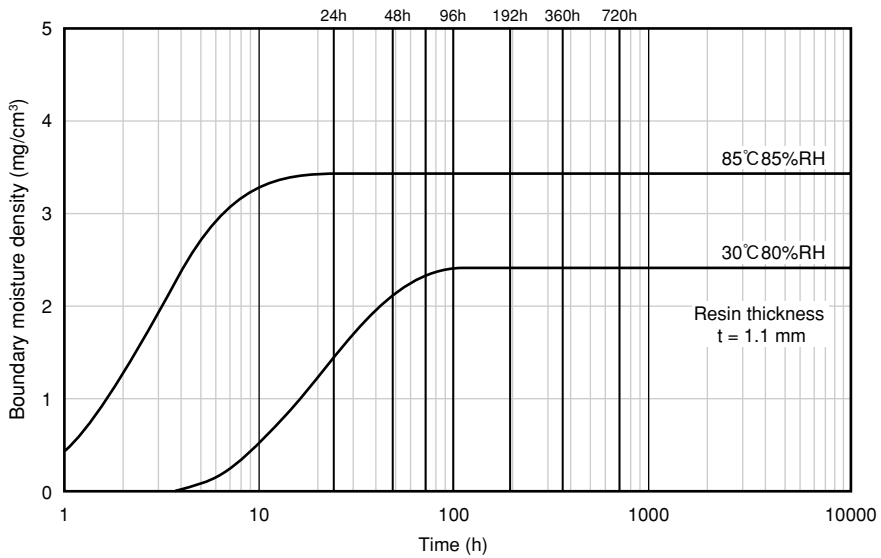


Fig. 5-6 Simulated Boundary Moisture Density Curves for a 28-pin TSOP

5.1.3 Evaluation Methods

5.1.3.1 Moisture Absorption Amount in Each Environment

Package moisture absorption environments are classified into three types as shown in Table 5-2. The first type is moisture absorption in the LSI assembly process; the second type is moisture absorption inside the moisture-proof packing, and the third type is moisture absorption in the mounting environment after opening the moisture-proof packing.

The Sony Semiconductor Network Company’s LSI assembly process indoor environment is controlled to $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ and $50\% \text{ RH} \pm 10\% \text{ RH}$. Therefore, moisture absorption simulations use the worst conditions of 28°C and $60\% \text{ RH}$.

The atmosphere inside moisture-proof packing is in a balanced state due to moisture exchange between the tray, package and desiccant. The moisture-proof packing used by the Sony Semiconductor Network Company is designed to achieve an internal relative humidity of $30\% \text{ RH}$ or less when placed in an ambient temperature of 30°C . Therefore, moisture absorption simulations assume conditions of 30°C and $30\% \text{ RH}$ inside the moisture-proof packing.

Customer mounting environments cannot be unconditionally determined, so 30°C and $70\% \text{ RH}$ are used as the worst environment.

Table 5-2 Atmospheres and Simulation Setting Conditions

	Assembly process	Inside moisture-proof packing	Mounting environment
Atmosphere	$25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ $50\% \text{ RH} \pm 10\% \text{ RH}$	30°C $30\% \text{ RH}$ or less	30°C $70\% \text{ RH}$ or less
Simulation conditions	28°C $60\% \text{ RH}$	30°C $30\% \text{ RH}$	30°C $70\% \text{ RH}$
Evaluation conditions	28°C $60\% \text{ RH}$	30°C $30\% \text{ RH}$	30°C $80\% \text{ RH}$

5.1.3.2 Moisture Absorption Amount Concepts and Settings for Evaluation

In the Sony Semiconductor Network Company’s assembly process, the moisture absorption time is controlled or baking is performed before shipment in accordance with the actual package cracking resistance of the device.

Fig. 5-7 and Fig. 5-8 show examples of boundary moisture density simulation curves used to evaluate these two cases.

There is significant variance in the time stored inside the moisture-proof packing, so the boundary moisture density after opening the moisture-proof packing is assumed to be the worst case. That is to say when the maximum boundary moisture density at the assembly process moisture absorption control time is greater than the saturation moisture density inside the moisture-proof packing, the value (1) in Fig. 5-7 is used as the initial value in the customer mounting environment. When baking is performed before shipment, the value (2) in Fig. 5-8 is used as the initial value.

Furthermore, 30°C and $70\% \text{ RH}$ are assumed to be the worst customer mounting environment, but the evaluation reference uses the boundary moisture density simulation curve for 30°C and $80\% \text{ RH}$ which provides a humidity margin of $10\% \text{ RH}$.

The boundary moisture density simulation curves in the mounting environment in Fig. 5-7 and Fig. 5-8 are used as the evaluation reference.

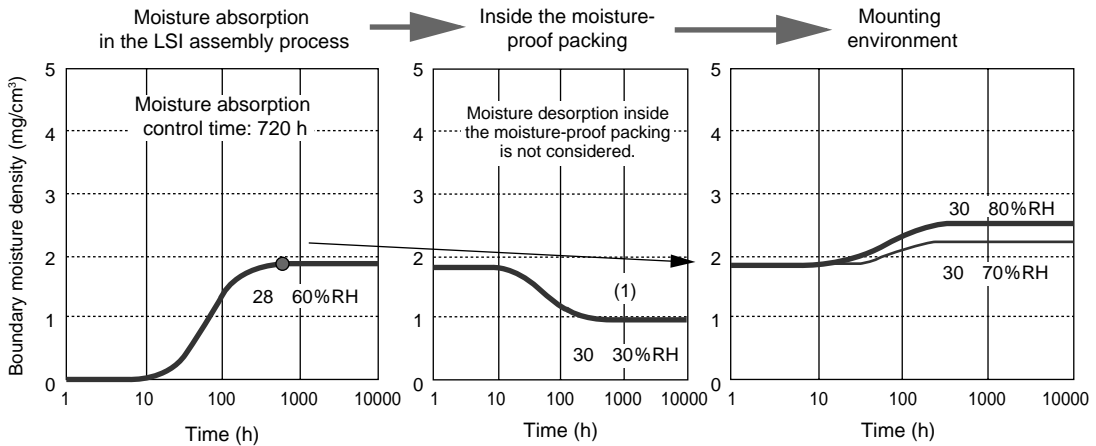


Fig. 5-7 100-pin LQFP Simulation Curve

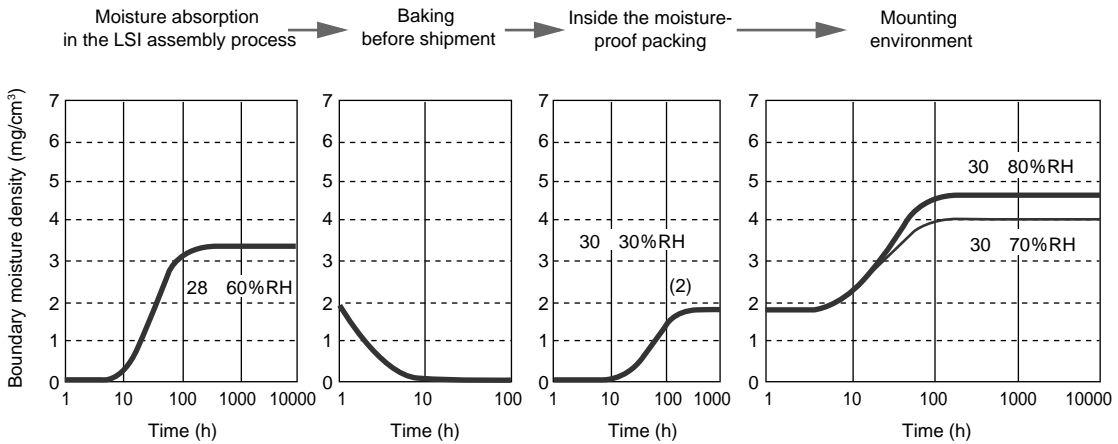


Fig. 5-8 20-pin SSOP Simulation Curve

5.1.3.3 Moisture Absorption Conditions for Evaluation

The moisture absorption conditions for evaluation sometimes use methods which accelerate moisture absorption at 85 °C to shorten the evaluation time. In addition, five relative humidity conditions from 45% RH to 85% RH are prepared to realize various boundary moisture densities, and acceleration is performed at the closest condition. Fig. 5-9 shows an example of this acceleration.

Table 5-3 shows the evaluation conditions for a 64-pin QFP package as an example.

For example, 8 days × 3 times is the condition where reflow is performed three times in 8 days or less. Here, moisture absorption at 30 °C and 80% RH for 192 h corresponds to moisture absorption at 85 °C and 55% RH for 48 h.

Also, Free × 3 times indicates evaluation which assumes three times in the saturation moisture absorption state in the mounting environment after opening the moisture-proof packing. Here, the moisture absorption conditions are 85 °C / 75% RH / 96 h, which are equivalent to the saturation moisture density of 30 mg/cm³ and 80% RH or more.

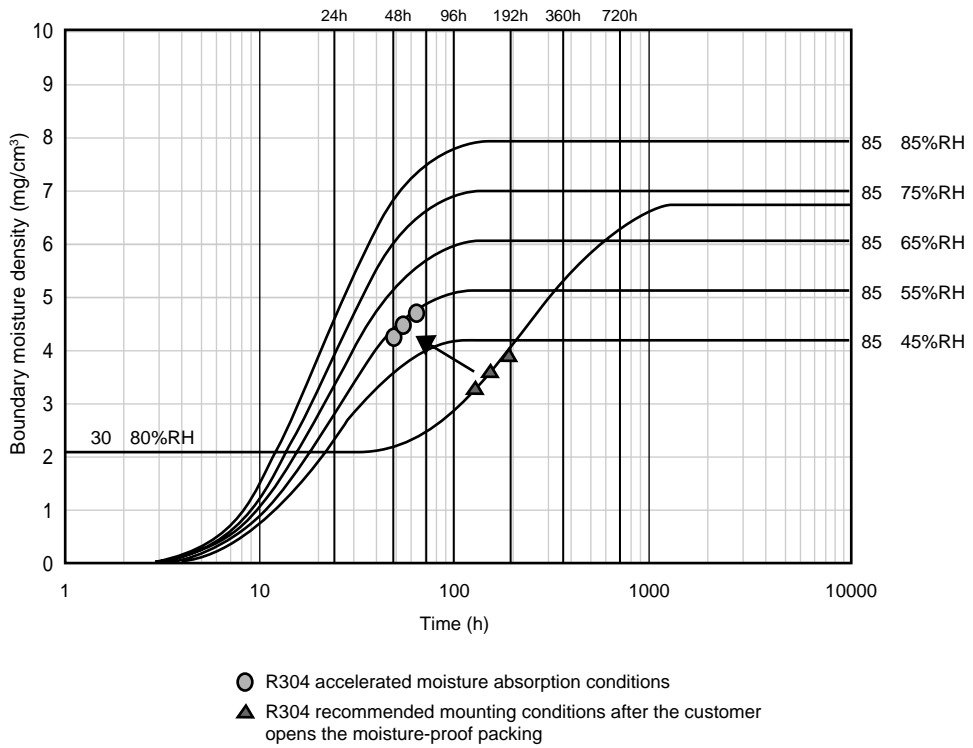


Fig. 5-9 64-pin QFP Moisture Absorption Condition Setting Simulation Curves

Table 5-3 Moisture Absorption Conditions for 64-pin QFP Evaluation

Operation limit	Moisture absorption conditions for evaluation	
	Temperature/Humidity	Time
2days × 3times (48h × 3times)	85 / 55%RH	24h
4days × 3times (96h × 3times)	85 / 55%RH	24h
8days × 3times (192h × 3times)	85 / 55%RH	48h
90days × 3times (2160h × 3times)	85 / 75%RH	96h

* The operation limit time is the time after opening the moisture-proof packing.

5.1.3.4 Evaluation Procedure

(1) Baking

The samples to be evaluated are first dried by baking, then moisture absorption is performed. Baking at 125 for 24 h or 125 for 48 h is selected according to the package to ensure complete drying.

(2) Moisture absorption

Moisture absorption is performed using the moisture absorption acceleration conditions set for each package and mounting rank.

(3) Heating

Fig. 5-10 shows the temperature profile for reflow heating. With the change to lead-free products, the reflow peak temperature was set at 260 max with three consecutive reflow times. The assured temperature and evaluation temperature are the same, but relative humidity is provided with a 10% margin. (assured humidity: 30 and 70% RH, evaluation humidity: 30 and 80% RH)

Also, the evaluation conditions for solder dipping are set at three consecutive dippings at 260 for 10 seconds to provide a relative humidity margin of 10% with respect to the assured conditions of 30 and 70% RH.

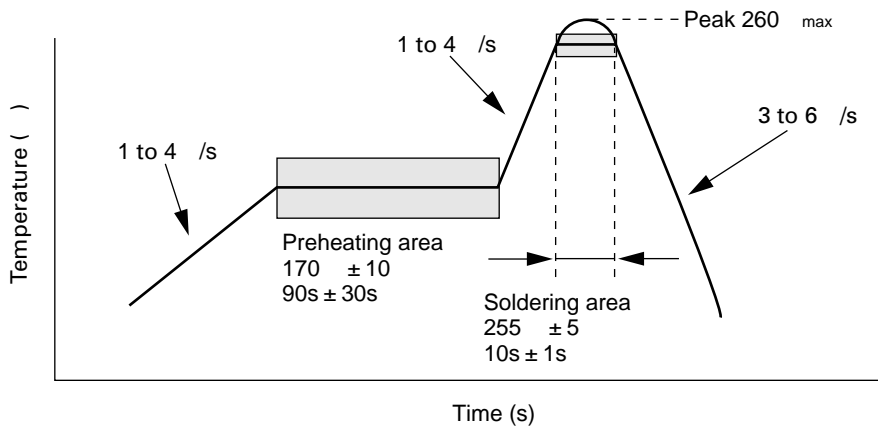


Fig. 5-10 Temperature Profile

(4) Judgment

The failure criteria are “significant delamination shall not be confirmed with scanning acoustic tomography (SAT),” “external and internal cracking shall not be confirmed in visual inspection of the exterior or cross section polishing,” and “failures shall not occur in continued reliability tests.”

5.1.4 Surface Mount Device Rank Assurance

The evaluation results in item 5.1.3 can be broadly grouped into 4 reflow ranks and 4 solder dipping ranks, and the mounting rank (package capability) is assured according to the combination of these ranks.

These mounting ranks are codified in the following manner and presented to customers as mounting codes.

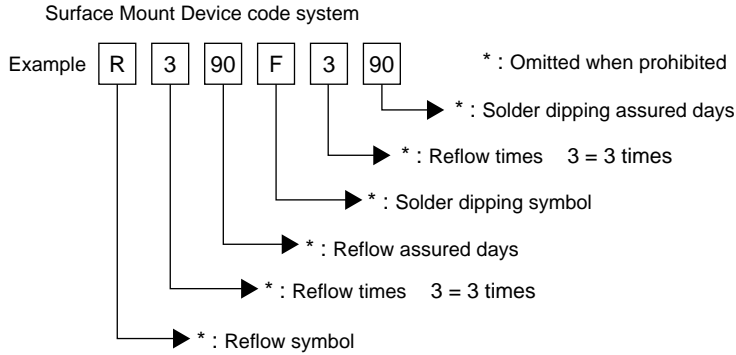


Table 5-4 shows a list of mounting codes. Note that the above example assures a storage limit of 90 days until the third reflow time after opening the moisture-proof packing. For solder dipping, the storage limit after opening the moisture-proof packing is 90 days.

Table 5-4 Surface Mount Device Code List

	SMD code		SMD code
1	R390F390	11	R304F390
2	R390F308	12	R304F308
3	R390F304	13	R304F304
4	R390F302	14	R304F302
5	R390	15	R304
6	R308F390	16	R302F390
7	R308F308	17	R302F308
8	R308F304	18	R302F304
9	R308F302	19	R302F302
10	R308	20	R302

5.1.5 Package Cracking Model

Environmental factors concerned with package cracking include the moisture absorption atmosphere and time, the solder heating method and number of times, and the heating temperature and time. With the recent diversification of mounting formats, these environmental factors are also being presented from customers in the form of various quality demands. In addition, higher heating temperatures due to the introduction of lead-free solder are becoming a large problem.

Under these circumstances, evaluation has been performed for individual mounting conditions thus far. However, this section describes a cracking model which allows simulation of cracking conditions without evaluation, and the results of verifying this model.

5.1.5.1 Package Cracking Model Concepts

Possible factors causing package cracking in evaluation of soldering heat resistance include boundary moisture density, maximum package temperature (heating peak temperature), heating time, and the number of heating times.

Tests were carried out to confirm these factors, and these results showed that the boundary moisture density and maximum package temperature factors have the largest effect.

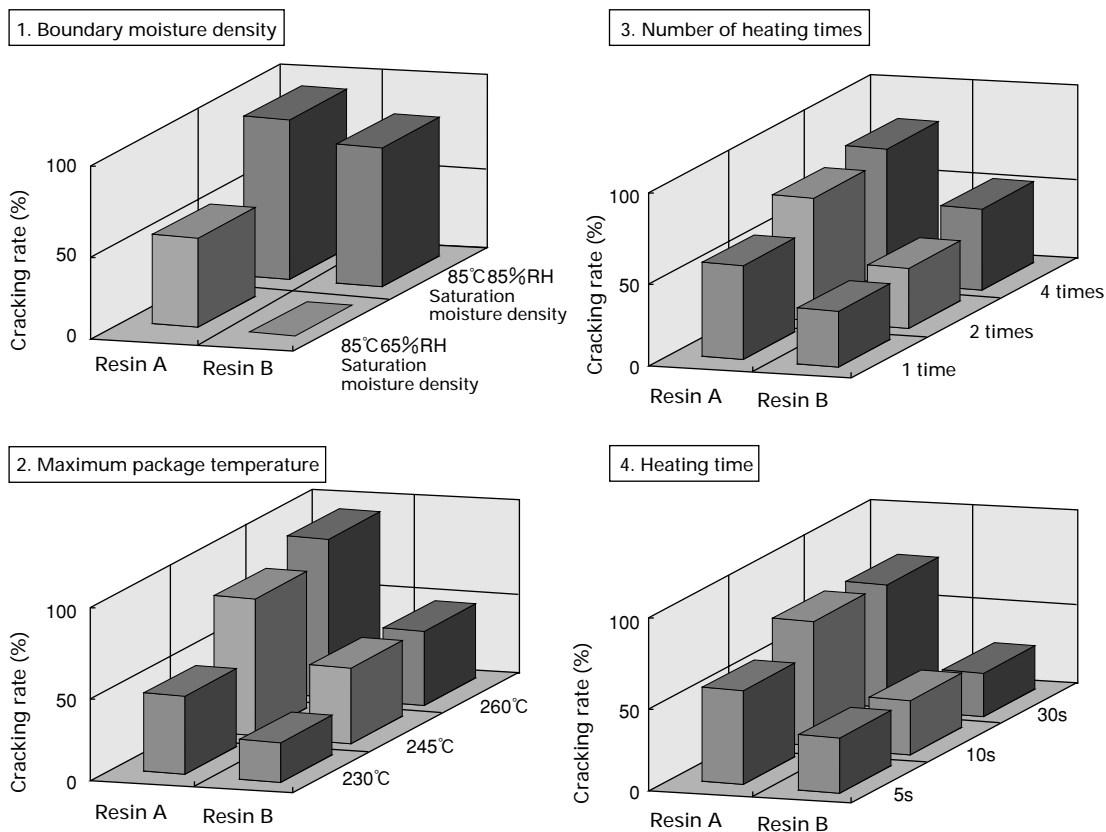


Fig. 5-11 Package Cracking Factor Confirmation Tests

As mentioned above, the main factors causing package cracking are the maximum package temperature and boundary moisture density. The package cracking conditions can be expressed by these two factors as shown in Equation 5-4.

$$Q > C \exp\left(\frac{Ea}{k \cdot T}\right) \quad 5-4$$

Where,
 Q : Boundary moisture density (mg/cm³)
 T : Maximum package temperature (K)
 C : Cracking constant
 Ea: Activation energy (0.4eV)
 k : Boltzmann's constant

This equation is the cracking model which represents the package cracking conditions.

The cracking constant C is an inherent package constant which is determined by the package structure unit. The package cracking conditions can be obtained through simulations by obtaining this constant beforehand.

Fig. 5-12 shows the basis for deriving this model.

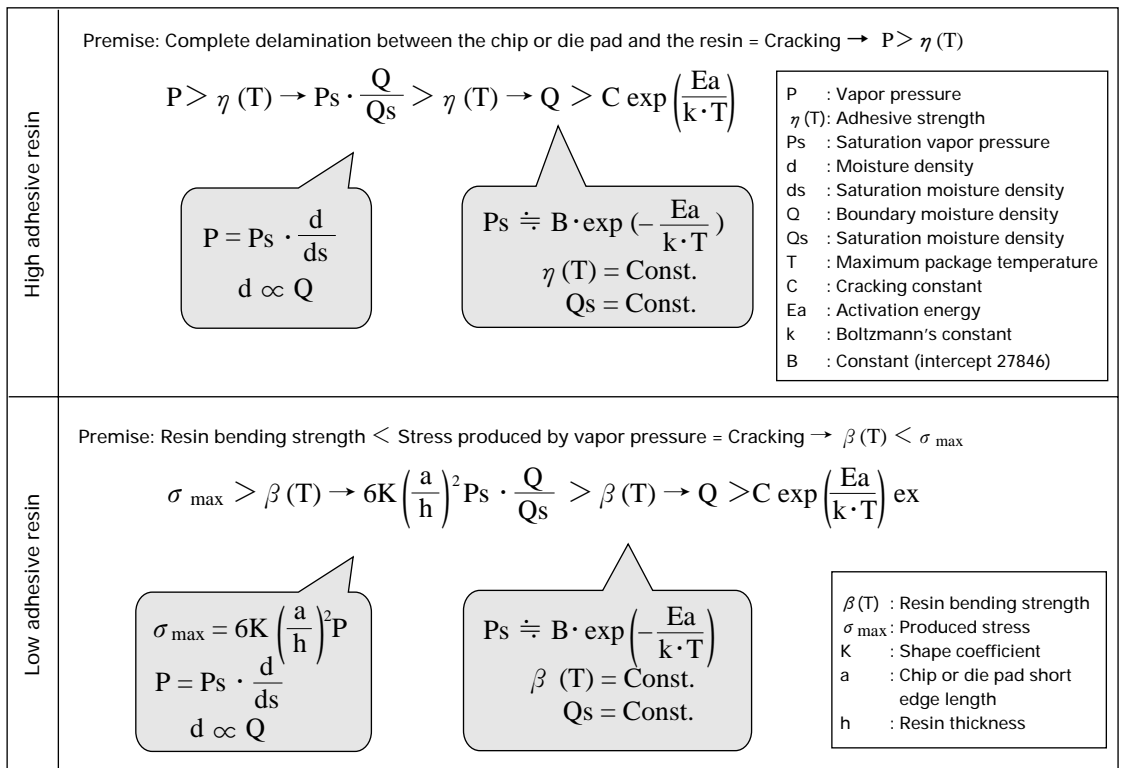


Fig. 5-12 Package Cracking Model

In addition, Fig. 5-13 and Fig. 5-14 show the results of verifying whether this model matches with the actual data. These figures show that this model can be accurately applied to actual data.

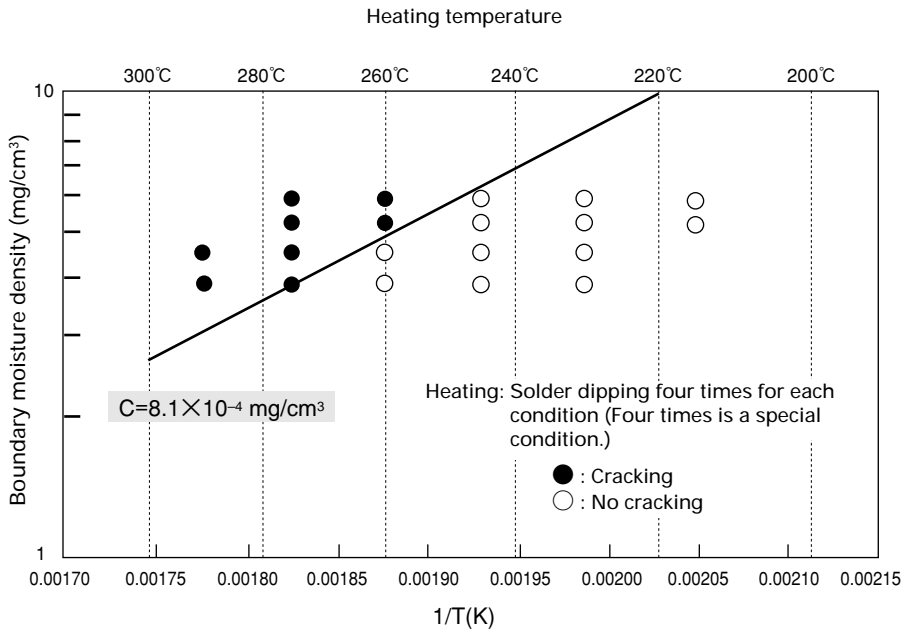


Fig. 5-13 100-pin LQFP (High Adhesive Plastic) Model Verification Test Results

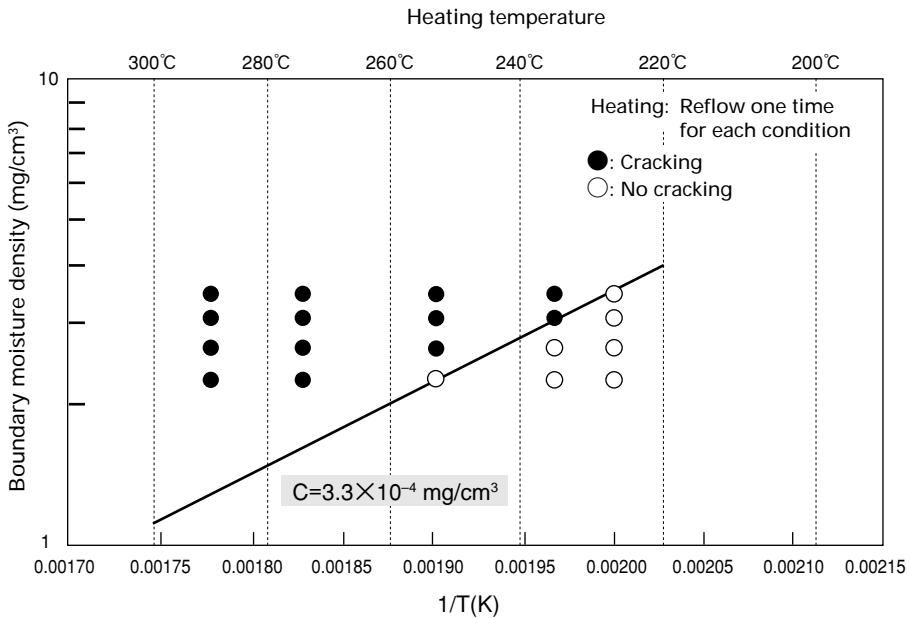


Fig. 5-14 100-pin QFP (Low Adhesive Plastic) Model Verification Test Results

5.1.5.2 Package Cracking Simulations

This section describes simulation of package cracking conditions using the package cracking model.

The cracking constant C for the 100-pin QFP package shown in Fig. 5-14 “100-pin QFP (Low Adhesive Plastic) Model Verification Test Results” is $3.3 \times 10^{-4} \text{ mg/cm}^3$. For example, let us consider how far the moisture absorption conditions (boundary moisture density) must be lowered to prevent package cracking when the maximum package temperature during mounting is raised to 260°C in order to change the soldering materials used during mounting to lead-free solder.

From Fig. 5-14, the limit boundary moisture density for a 100-pin QFP package at a maximum package temperature of 260°C is 2.0 mg/cm^3 . Thus, package cracking can be prevented by keeping the boundary moisture density below this limit.

Fig. 5-15 shows the moisture absorption simulation curve for this package.

The boundary moisture density can be kept to 2.0 mg/cm^3 or less and package cracking can be suppressed by mounting within 10 days after opening the moisture-proof packing.

In this manner, the package cracking conditions can be obtained using the package cracking model and moisture absorption simulations.

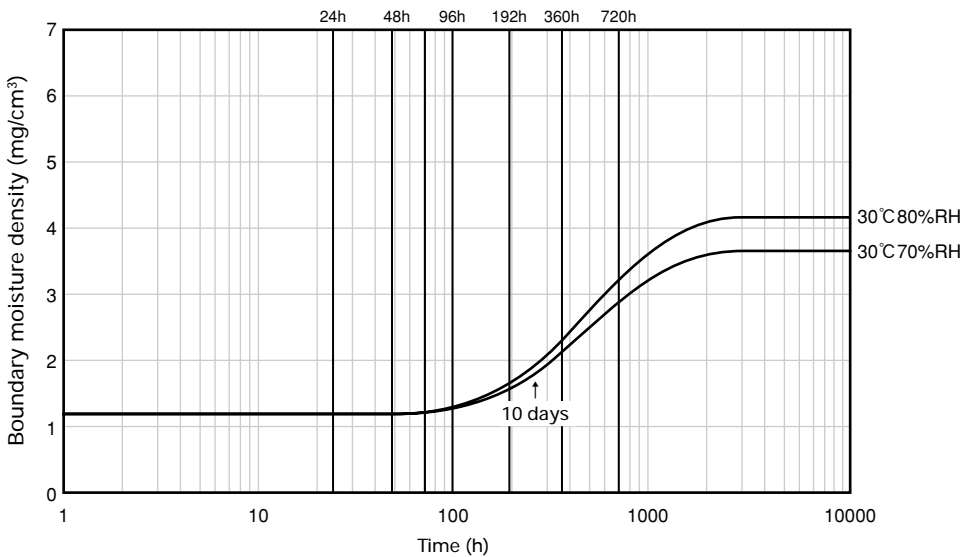


Fig. 5-15 100-pin QFP Moisture Absorption Simulation Curve

5.1.5.3 Evaluation of Capability

The package cracking capability is determined by the cracking constant C , and the capability evaluation procedure for obtaining this constant is as follows.

(1) Baking

The samples to be evaluated are first dried by baking, then moisture absorption is performed. Baking at 125°C for 24 h or 125°C for 48 h is selected according to the package to ensure complete drying.

(2) Moisture absorption

Moisture absorption is performed under the conditions shown in Table 5-5. The diffusion rate of moisture varies depending on the resin, so the saturation time for the two conditions shown in Table 5-5 may be set according to the diffusion and solubility coefficients.

Table 5-5 Moisture Absorption Conditions

Temperature and humidity	Moisture absorption time for each package thickness (t mm)		
	t ≤ 1.4	1.4 < t ≤ 2.0	2.0 < t
Condition 1: 85 °C 65%RH	48h	96h	168h
Condition 2: 85 °C 85%RH	48h	96h	168h

(3) Heating

Heating is performed by reflow or solder dipping. The respective conditions are shown below.

Reflow: Profile Conforms to Fig. 5-10.

Peak temperature Five conditions of 240 °C, 250 °C, 260 °C, 270 °C and 280 °C

Solder dipping: Dipping time for each package thickness

t ≤ 1.4mm	15s
1.4mm < t ≤ 2.0mm	30s
2.0mm < t	40s

Solder temperature Five conditions of 240 °C, 250 °C, 260 °C, 270 °C and 280 °C

The number of samples is n = 10 for each temperature condition.

(4) Judgment and calculation of cracking constant C

The failure criteria are “significant delamination shall not be confirmed with scanning acoustic tomography (SAT),” “external and internal cracking shall not be confirmed in visual inspection of the exterior or cross section polishing,” and “failures shall not occur in continued reliability tests.”

Note that cracking constant C is calculated using Equation 5-4 based on the worst conditions under which cracking does not occur.

<References>

- 1) Kansai Electronic Industry Development Center, Reliability Subcommittee, “Survey Report of Documents Concerning the Pressure Cooker Test” (1983)
- 2) Nanjo, “Materials and Moisture Handbook”, Society of Polymer Science, Polymer and Moisture Absorption Committee (1968)
- 3) J.Krank: “The Mathematics of Diffusion”, Oxford Univ. Press, London, (1956).
- 4) Etoh, Kayama, Sasaki, “A Study on SMD Soldering Heat Resistance Evaluation Methods”, RCJ Reliability Symp. (1997)

5.2 Notes on Handling for Electric Breakdown

The resistance of semiconductor devices to overvoltages, overcurrents, noise and other electrical stress is dropping due to the miniaturization of elements and wiring. Even slight voltage fluctuations or noise which were not a problem thus far are becoming increasingly likely to cause device misoperation or breakdown. This section describes countermeasures to prevent semiconductor devices from misoperating or breaking down due to electrical stress.

5.2.1 Electrostatic Breakdown

The gate oxide film thickness of MOS transistors manufactured using the latest processes has already been reduced to 5 nm or less, and the endurance voltage of these oxide films is only several voltage. Semiconductor devices employ countermeasures such as circuits to protect against the entry of external static electricity for each input/output pin to prevent static electricity from being applied to the internal transistors. However, if the transistor endurance voltage drops to several voltage or less, it becomes extremely difficult to reduce external static electricity in excess of several 100 V to the transistor endurance voltage or less using only protection circuits.

Furthermore, as device operating speeds increase, the effect of the parasitic impedance of protection circuits on operating speed cannot be ignored, and an increasing number of pins are unable to obtain the required characteristics without reducing the size of these protection circuits or eliminating them altogether. As device miniaturization and increases in operating speed progress further, it is thought that the electrostatic endurance voltage of the devices themselves will drop rapidly.

Against this background, countermeasures for preventing electrostatic breakdown are becoming even more important in processes where semiconductor devices are handled. General knowledge required to protect semiconductor devices from electrostatic breakdown during handling, methods for controlling static electricity within processes, and countermeasures against electrostatic breakdown are described below.

5.2.1.1 Basic Electrostatic Discharge Control Concepts

Basic concepts for electrostatic discharge controls in processes where semiconductor devices are handled are as follows.

- (1) Designing processes and facilities which do not generate static electricity
- (2) Not bringing items which are easily charged by static electricity into processes
- (3) Quickly dispersing static electricity which does occur to prevent discharge
- (4) Periodically checking electrostatic discharge control conditions and maintaining countermeasure effects
- (5) Instilling an awareness of the need for electrostatic countermeasures in workers and process controllers

(1) Designing processes and facilities which do not generate static electricity

During process design or when investigating the introduction of manufacturing facilities, processes with effective electrostatic discharge controls can be constructed by introducing electrostatic discharge control facilities (grounds, floors, environment, etc.) and building countermeasures for preventing the generation of static electricity by friction or contact into the equipment specifications.

(2) Not bringing items which are easily charged by static electricity into processes

Electrostatic breakdown due to triboelectric charging or inductive charging can be prevented by not bringing packing materials, paper, fixtures, office supplies or other insulated objects which easily generate static electricity into processes except when absolutely necessary.

(3) Quickly leaking static electricity which does occur to prevent electrostatic discharge

Chances for electrostatic discharge (ESD) to semiconductor devices can be reduced by quickly leaking generated static electricity using methods such as grounding equipment and jigs, controlling resistance values on floors and work surface, and neutralizing charges with an ionizer. In addition, charges can be gradually leaked without causing sudden discharge and electrostatic breakdown can be prevented by changing metal parts which contact devices to materials with appropriate resistance values.

(4) Periodically checking electrostatic discharge control conditions and maintaining countermeasure effects

After implementing electrostatic countermeasures, the effects of these countermeasures cannot be maintained unless periodic checks are made and control is performed to ensure that the effects are reliably maintained.

(5) Instilling an awareness of the need for electrostatic discharge controls in workers and process controllers

Electrostatic discharge controls require knowledge and understanding of static electricity on the part of employees working in processes and process controllers. Electrostatic protective items can be even more effective at preventing electrostatic breakdown depending on the awareness of the person using them.

Electrostatic discharge controls are not a problem which can be solved simply by introducing electrostatic protective items. Ensuring thorough and consistent countermeasures and spreading general knowledge of electrostatic discharge control concepts can make process managers and workers aware of the risk of electrostatic breakdown, and is an effective means of reducing electrostatic breakdown problems within processes.

5.2.1.2 Approach toward Process Control References

In order to control electrostatic charge levels within processes, it is necessary to determine the charge level to use as the control criteria. This control reference is set based on the ESD withstand voltage of the devices handled in that process. However, among the electrostatic breakdown testing models for devices described in item 2.4.6.3, which testing method should be used to obtain the ESD withstand voltage employed as the process control reference guideline is an important issue in determining this control reference. Even if control criteria are set based on ESD phenomena which do not occur in the process, this does not necessarily mean that actual electrostatic breakdown can be effectively prevented.

Fig. 5-16 shows the relationship between charged objects present in processes and electrostatic capacity. Objects causing ESD within processes generally have different electrostatic capacity. For example, the electrostatic capacity of the human body is usually said to be approximately 80 to 200 pF^{1) 2) 3) 4)}, which is equivalent to the capacitance used by the human body model (HBM). In contrast to this, most items other than workers which may produce ESD with devices such as tweezers and metal parts on chip mounters such as device adsorption jigs and positioning stages have electrostatic capacity of only several pF to several 10 pF.⁴⁾ In addition, the electrostatic capacity of most semiconductor devices is also mostly within the range of several pF to several 10 pF. (Table 5-6) When the electrostatic capacitance of charged objects becomes smaller in this manner, the accumulated electrostatic energy is lower even when charged to the same voltage, so semiconductor devices are less likely to experience electrostatic breakdown.

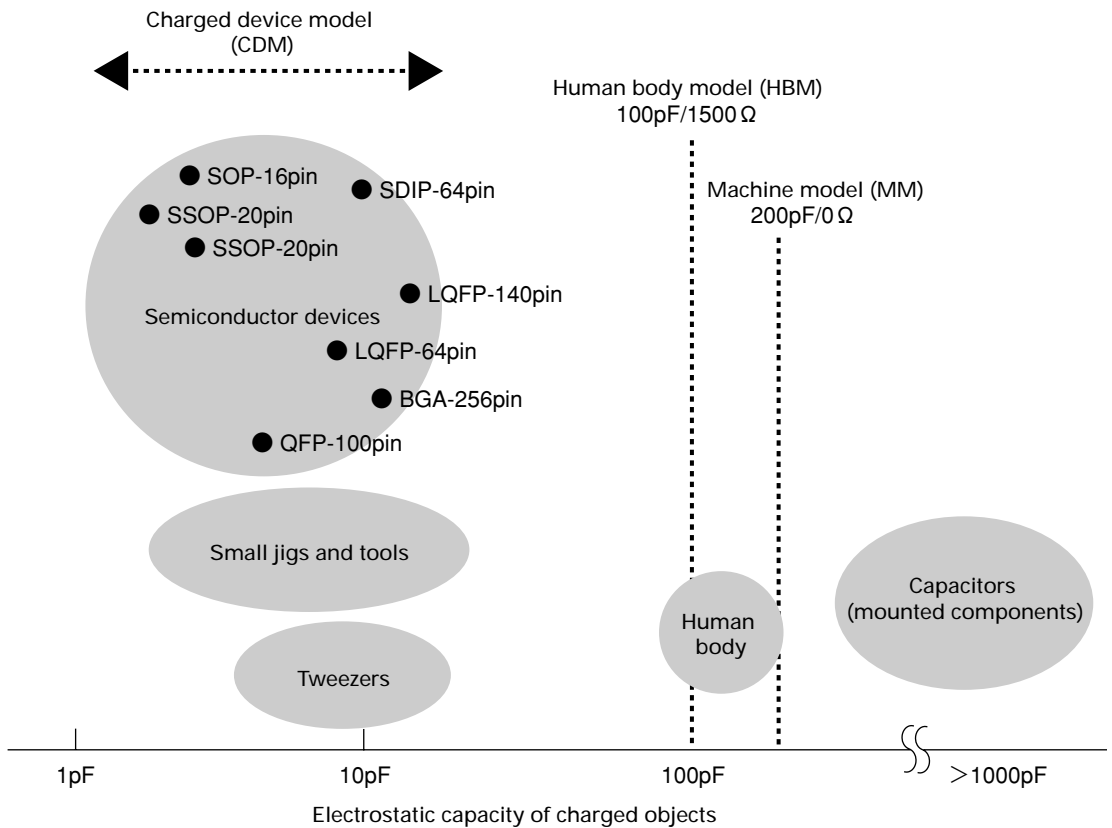


Fig. 5-16 Relationship between Charged Objects in Processes and Testing Methods from the Viewpoint of Electrostatic Capacity

Table 5-6 Device Package Electrostatic Capacity Measurement Results (when placed on a metal plate with the leads facing upwards)

Package	Electrostatic capacity (pF)	Package	Electrostatic capacity (pF)
SSOP-20pin	2.0	QFP-100pin	5.6
SOP-16pin	3.7	LQFP-140pin	13.2
LQFP-64pin	7.4	BGA-119pin	9.5
SDIP-64pin	10.5	BGA-256pin	10.6

It has been reported that failure modes produced by the discharge of static electricity accumulated in small electrostatic capacity clearly differ in most cases from failure modes when static electricity is discharged from the large capacitances (100, 200 pF) used in HBM and MM tests.^{(6) (7) (8)} As seen in Fig. 5-16, the charged device model (CDM) testing method which uses the parasitic capacitance of the device itself is thought to be the most suitable testing method for reproducing phenomena where static electricity is discharged from small capacitance charged objects within processes.^{(6) (8) (9) (10)}

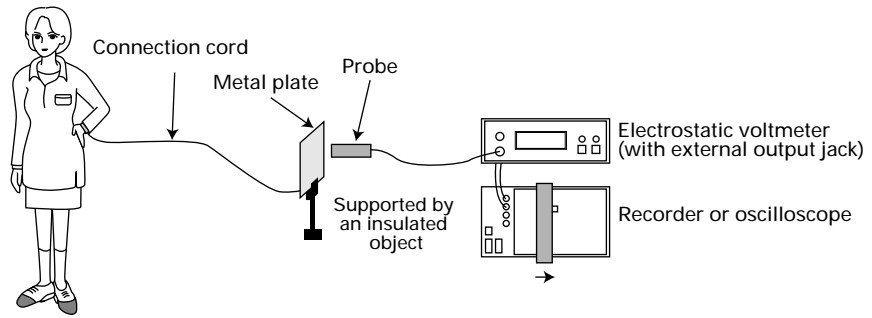
In this manner, an appropriate charge level control value for charged objects within processes should be set according to the type of charged object. Thus, it is thought that more realistic charge level control criteria can be achieved by using ESD withstand voltage data from the human body model (HBM) as a reference for workers (human bodies), and ESD withstand voltage data from the charged device model (CDM) as a reference for devices and jigs.

5.2.1.3 Basic Electrostatic Discharge Controls^{(11) (12)}

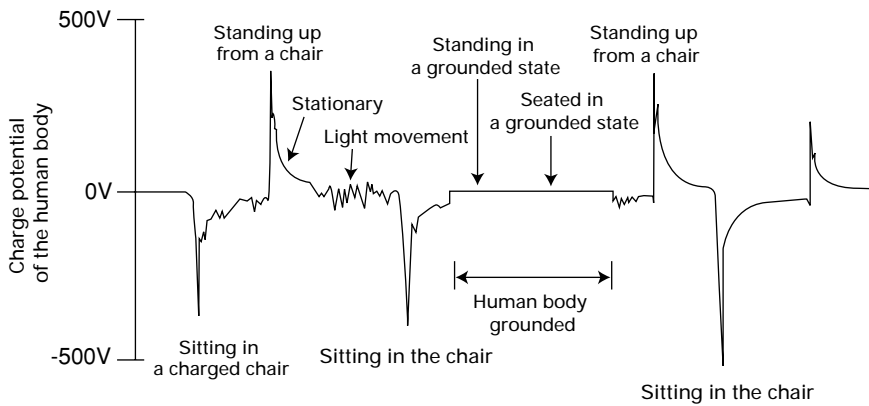
(1) Countermeasures for the human body

Workers who directly handle semiconductor devices or substrates on which devices have been mounted should wear both wrist straps and ESD protective shoes. The charge potential of the human body varies greatly according to worker movements, and the charge potential may rise sharply due to a motion such as standing up from a chair. (Fig. 5-17) Stable charge removal performance can be obtained by wearing a wrist strap adhered closely to bare skin, but the cord may be severed if a sudden load is placed on the cord during the work. If the soles of ESD protective shoes become dirty, the contact resistance between the human body and the floor increases and the prescribed leak resistance may not be obtained. Also, if a worker sitting in a chair places both feet on a footrest or other pedestal, conductivity between the floor and the human body is not obtained and the constantly required electrostatic leakage effects cannot necessarily be maintained. Therefore, safety can be most effectively assured by having workers who directly handle devices wear both wrist straps and ESD protective shoes.

Gloves and finger sacks with ESD protection should be used. In particular, the finger sacks used when handling devices with bare hands must be conductive. If the surface of finger sacks becomes charged, an electrostatic charge is induced in the device when a device is held, and the risk of the charged device model (CDM) discharge phenomenon occurring increases. (Fig. 5-18, Fig. 5-19)



(a) Measurement method



(b) Measurement results

Fig. 5-17 Changes in the Charge Potential of the Human Body

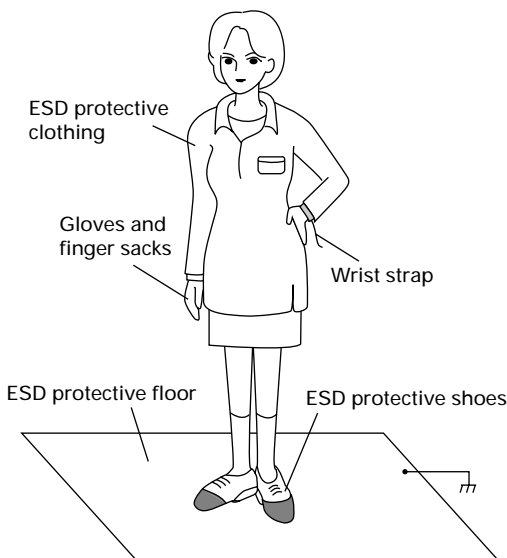


Fig. 5-18 Human Body (Worker) Countermeasures

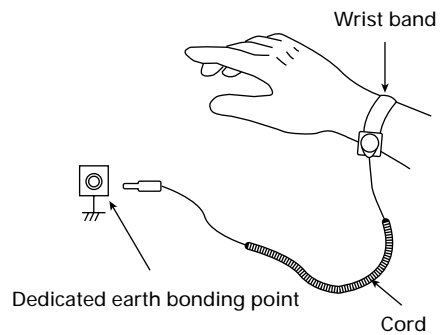


Fig. 5-19 Wrist Strap Usage

(2) Work surface

Work surfaces should be covered with ESD protective sheets (made from conductive materials or materials having electrostatic dissipative characteristics) or work tables should be made from materials having these same characteristics. Also, work surfaces must be grounded. (Fig. 5-20) Insulated objects which easily generate static electricity should not be placed on work surface. Fixtures and jigs required for work should be made from conductive or electrostatic diffusive materials, or ionizers should be used when that is not possible. The use of insulated objects for items which may contact or approach devices should be avoided as much as possible, especially during work. Also avoid working with insulated sheets or plates on worktables.

The seat and back rest surfaces of chairs that workers sit in should have ESD protective covers, or ESD protective chairs should be used. (Fig. 5-21) As shown in Fig. 5-17, static electricity with an extremely high potential may be generated momentarily when standing up from a chair.

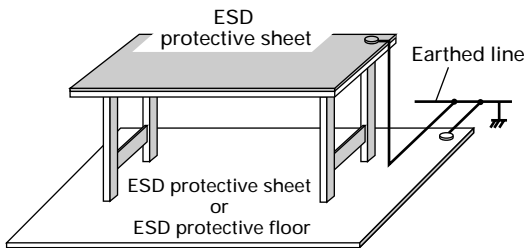


Fig. 5-20 Work surface

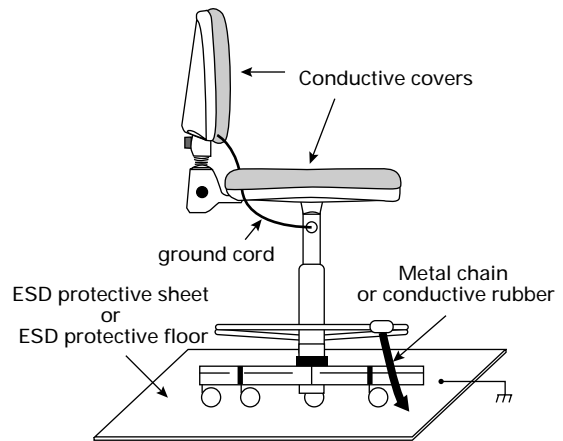


Fig. 5-21 Chair

(3) Floor

Floors in the work area should be ESD protective floors or covered with ESD protective sheets. When the entire work area floor cannot be covered, at the very least lay ESD protective sheets in the work area where workers wearing ESD protective shoes handle devices or substrates on which devices have been mounted. When laying ESD protective sheets, be sure to ground all of the sheets. (Fig. 5-20)

(4) Equipment and facilities

The frames of equipment such as mounters, solder baths and measuring instruments, and facilities such as belt conveyors must be grounded. (Fig. 5-22) Metal parts which are isolated from the grounded frame by insulating material and which may contact devices should be grounded individually. Insulating material parts which may contact or approach devices should be changed to materials with electrostatic dissipative characteristics, or charges should be eliminated using ionizers.

Both the body and tips of electric screwdrivers, soldering irons and other tools should be grounded. Otherwise, electric over stress (EOS) breakdown may occur if there is an AC voltage leak.

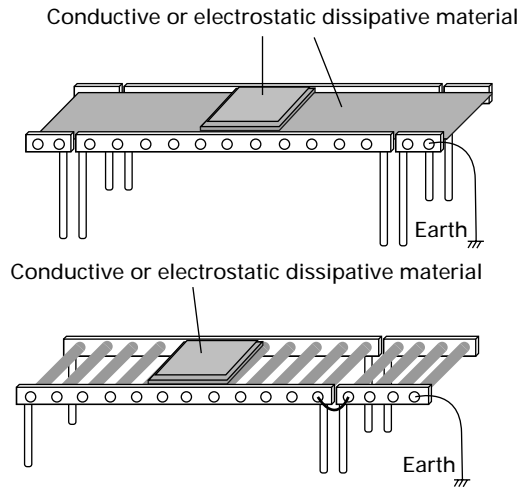


Fig. 5-22 Belt Conveyor

(5) Environment

It is generally considered difficult for static electricity to occur at higher humidity (moisture density in the air). However, rather than static electricity being difficult to generate, what actually happens is that the proportion of the generated charge that leaks due to moisture adhered to the surface increases, with the result that charging appears difficult. In process humidity control it is important to maintain a humidity environment which makes it difficult for static electricity to occur. In actual processes, however, heat generation by equipment and other factors create spaces with locally high temperatures (low relative humidity). Furthermore, substrates which generate heat when the power is on, components packed in plastic trays and bags, and products stored for long periods inside dry warehouses may not necessarily always be in a condition which inhibits the generation of static electricity. Therefore, it is extremely dangerous to think that static electricity can be uniformly inhibited by increasing the humidity, or that other electrostatic discharge control can be omitted. Humidity environment control must be understood only as an auxiliary electrostatic control.

(6) Storage and transport

Semiconductor devices should be stored in the packing format for shipment. Correctly storing devices in the same ESD protective packing materials as when shipped reduces the risk of electrostatic breakdown even when devices are handled during storage.

In addition, substrates on which devices are mounted must be stored in containers or on storage shelves made from conductive or electrostatic dissipative material. (Fig. 5-23, Fig. 5-24) At this time, the use of insulated partitions or storage in plastic insulated bags should be avoided. Mounting substrates are made from insulating materials, so if substrates become charged by vibration or rubbing during storage or transport or if they are placed near charged objects, an inductive charge may be generated in the substrate wiring pattern, and may discharge from the connectors during measurement or assembly and damage the device.

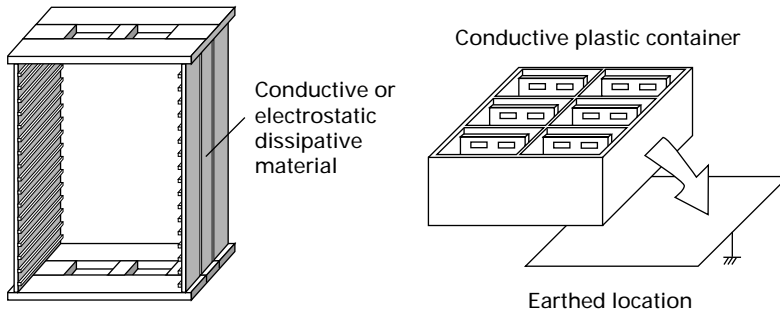


Fig. 5-23 Board Storage Container

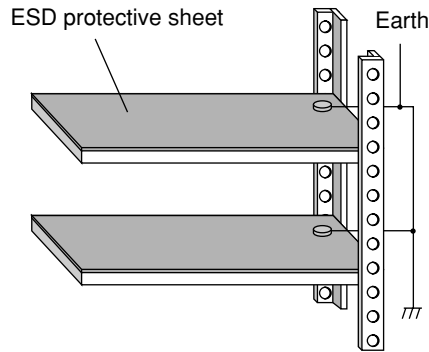


Fig. 5-24 Storage Shelf

(7) Components other than devices

Many components other than semiconductor devices which are mounted on boards become electrostatically charged during board mounting. Components such as condensers, LCD pannels and flexible connectors which have capacitances capable of accumulating static electricity may cause ESD during board mounting and damage devices.

Parts boxes used to store these components and delivery packing must have electrostatic countermeasures. (Fig. 5-25) Workers should be aware that some mounted components other than devices can also carry electrostatic charges, and countermeasures must be taken to prevent these components from causing ESD during board mounting.

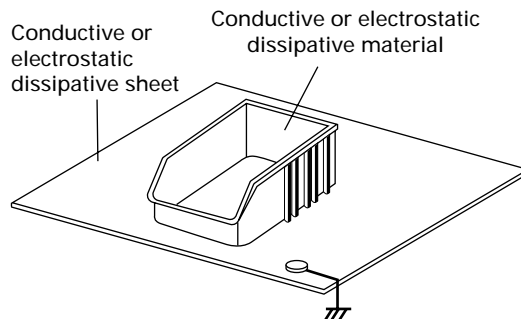


Fig. 5-25 Parts Box

(8) Eliminating charges using an ionizer

Ionizers are charge elimination equipment which generate corona discharge by applying a high voltage to the tip of a discharge electrode, and neutralize static electricity with the generated ions. Ionizers are an effective means of eliminating static electricity from insulating material which cannot be discharged by grounding. Unlike charges on metal, there is no risk of charges on insulating material being discharged to and damaging devices. However, these charges may generate inductive charges in devices and metal parts. Ionizers are effective when using insulating material near devices.¹³⁾

(9) Clothing

Workers should make efforts to wear clothing made from materials which do not generate static electricity. Clothing made from materials which easily generate static electricity may induce strong static electricity in human bodies with movement.

(10) Characteristics required of ESD protective items

The values given in the table below are references for the characteristics required of main ESD protective items. Even when the characteristics noted in the Specifications satisfy the required standards, the effects should be thoroughly verified before selecting ESD protective items for introduction.

Table 5-7 Characteristics Required of Main ESD Protective Items¹⁴⁾

ESD protective item	Surface resistivity R_s ($\Omega \cdot \text{cm}$) Resistance R_p (Ω)	Resistance value to GND R_g (Ω)
Floor	—	$< 1 \times 10^9$
ESD protective sheet	$1 \times 10^4 < R_s < 1 \times 10^{10}$	$1 \times 10^5 < R_g < 1 \times 10^9$
ESD protective shoes (when worn)	—	$5 \times 10^4 < R_g < 1 \times 10^8$
Wrist strap (cord)	$7.5 \times 10^5 < R_p < 5 \times 10^6$	—
Wrist strap (when worn)	—	$5 \times 10^4 < R_g < 1 \times 10^8$
Chair	—	$< 1 \times 10^{10}$

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- 10) Fukuda et al., "Electrostatic Breakdown Testing Method for Semiconductor Devices Using the Charged Device Model", IEICE CMP-86-133, pp.37 (1997)
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- 12) "Report on the Results of Investigative Findings on the Standardization of Device ESD Resistance Tests", Reliability Center for Electronic Components of Japan (1994)
- 13) "Utilization Guide for Ionizers Used at Semiconductor Device and other Production Sites", Reliability Center for Electronic Components of Japan (1995)
- 14) IEC 61340-5-1 (1998)

5.2.2 Strong Electric and Magnetic Fields

Strong external electromagnetic fields are generally not the direct cause of device failure. However, when devices are exposed to strong magnetic fields, the impedance may change, the leak current may increase, or other abnormal phenomenon may occur due to polarization of the package plastic materials or inside the IC chip.

In addition, if power supplies or parts which generate high voltages are located near devices, large noise in the power supply or ground lines may cause circuits to misoperate or the IC to generate noise.

To prevent these external electromagnetic interferences from impeding circuit functions, circuit layout patterns and component arrangements on printed substrates are optimized and shielded wires are used. In addition, care must be given to the set design such as changing mounting locations or providing electric and/or magnetic field shielding as necessary.

5.2.3 Overvoltage Breakdown (EOS Breakdown)

Failure modes where overvoltage or overcurrent other than static electricity causes breakdown are called overvoltage breakdown or electric over stress (EOS) breakdown. Electric over stress has various causes, but device failure is generally caused by the application of pulse type electric over stress called surge. Causes of surge include equipment power-on/off, relay switching, discharge from capacitive loads, lightning surge due to lightning strikes, etc.

The surge-induced EOS breakdown mechanism differs according to the type of applied surge, but applying voltage in excess of the ratings to the device power supply or input/output pins causes junction breakdown inside the device or the phenomenon where parasitic transistors are activated. At this time, if an overcurrent flows and the energy consumed by the aluminum wiring and transistors exceeds the wiring or junction endurance level, the wiring may melt or junctions may suffer thermal breakdown.

Countermeasures against EOS breakdown include inserting voltage clamp diodes or capacitors to the power supply and input/output pins on the substrate to prevent surges from entering the inside of the substrate. In addition, noise countermeasures must also be taken for measuring instruments used to adjust substrates within processes.

5.2.4 Handling of High Frequency Devices

As semiconductor devices incorporate more advanced functions and performance, the device structures are being further miniaturized with higher densities, and oxide films and wiring layers are becoming thinner. This has resulted in an intrinsic drop in electrostatic strength.

To increase the electrostatic strength, countermeasures such as adding electrostatic protection circuits to device input/output pins are generally taken, but this also has the drawback of causing characteristics degradation.

Particularly for high frequency and high speed devices, adequate electrostatic countermeasures cannot be taken for some pins in order to satisfy the required performance.

Therefore, thorough countermeasures must be taken in all aspects from device storage and transport to set mounting, inspection and other work environments, and also for handling during work.

5.2.5 Latch-up

Latch-up is the phenomenon where overvoltage or current stress such as static electricity or noise entering from an external source triggers the parasitic thyristors in CMOS devices and creates a short circuit between the power supply and GND.

The latch-up phenomenon occurs in the operating condition (the condition with the supply voltage applied), but as long as voltage stress which exceeds the device ratings is not applied, there is little or no risk of latch-up occurring within the normal operating voltage range. Latch-up which occurs randomly while using electronic equipment is thought to be mostly caused by the entry of stress in excess of the ratings to products incorporating semiconductors or the occurrence of this type of situation during operation. Possible causes of latch-up are as follows.

(1) Entry of static electricity from an external source

When static electricity enters an operating device which is mounted on a substrate, the discharge current passes through the input/output pin protective elements and flows to the power supply or GND wiring. In consideration of discharge from human bodies, the peak current value that flows at an ESD of several kV can reach several A to several ten A. If this current flows to the substrate power supply or GND wiring, the power supply or GND potential fluctuation may reach several V and exceed the device ratings. If this voltage fluctuation occurs during device operation, the junctions inside the device may break down and cause latch-up.

Portable electronic equipment (cellular phones, camcorders, laptop computers, portable data terminals, digital cameras, etc.) have spread rapidly in recent years, and the frames of these electronic equipment which are frequently and directly touched by people are not grounded. Therefore, these equipment are easily affected by supply voltage fluctuations caused by ESD from human bodies, and have a high risk of latch-up. Furthermore, in order to achieve higher speeds, compact size and low power consumption, these products use many devices manufactured by the latest processes, so the voltage margin against latch-up is becoming even stricter due to lower supply voltages and junction withstand voltages.

(2) Entry of lightning surge

Semiconductor devices used in communications facility or power supply facility equipment may experience latch-up due to lightning surge entering via communication cables or transmission lines. Household electronic products may also experience latch-up due to lightning surge entering through utility poles, transmission cables or telephone lines, etc.

(3) Electromagnetic susceptibility (EMS)

If sources of electromagnetic noise (car engines, cathode ray tubes, ESD) are present around electronic equipment, noise induced by sudden changes in the electromagnetic field may cause latch-up.

(4) Live wire insertion or removal

When performing maintenance or repair work on operating systems, depending on the manner in which the connectors are connected, voltage may be applied to the input/output pins before power is supplied to the substrate when a substrate is inserted with the system in the operating condition. At this time, the input/output pin potential momentarily becomes higher than the supply voltage, causing an influx of current from the pin and resulting in latch-up.

(5) Supply voltage application sequence for multi-power supply devices

In devices with multiple different power supplies, the potential of certain pins may rise above the supply voltage depending on the sequence in which the supply voltages are applied, and this may cause latch-up. Care must be taken for the order in which the power supplies are applied to the device for devices which use multiple power supplies.

Latch-up caused by these types of external factors can be suppressed by taking countermeasures to prevent the entry of surges and noise which serve as the respective triggers. Effective countermeasures for static electricity or surges which directly enter devices include inserting surge countermeasure diodes, capacitors or other elements to the substrate entrances which are the entry routes, or using substrate power supply and GND wiring patterns which are resistant to potential fluctuations and noise. In addition, lowering the power supply and GND wiring impedance, suppressing potential fluctuations due to sudden currents, and separating the power supply and GND wiring of circuit blocks which are susceptible to external surges from other circuits are also effective countermeasures. Countermeasures for the power supply application order include inserting capacitors or taking other measures to delay the respective rise timings, etc.

Electromagnetic noise requires shielding countermeasures to prevent electromagnetic waves from entering electronic equipment or the use of wiring patterns which are resistant to induction by electromagnetic fields. When sources of electromagnetic noise are present inside equipment, countermeasures must be taken for the noise source or the power supply and GND wiring must be separated, etc.

5.2.6 Thermal runaway

Thermal runaway is the phenomenon where positive feedback increases the power due to the temperature characteristics of the IC internal circuits, causing the temperature to rise without limit and resulting in failure. Most failure after mounting is thought to be caused by thermal runaway. In addition to thermal runaway caused by local heat generation in the device, thermal runaway may also occur depending on the heat radiation structure in power devices. Therefore, special care must be given to heat radiation design.

5.3 Notes on Handling for Mechanical Breakdown

Devices should be handled carefully. Devices may be damaged by dropping or shocks, so care should be taken to keep mechanical vibrations and shocks to a minimum.

Devices are comprised of chips, bonding wires, external pins, radiation fins, mold resin and other elements, and the mechanical strength and coefficient of thermal expansion of each component material differ. Therefore, mechanical breakdown may occur in various cases such as when forming or cutting external pins, mounting devices on printed substrates, washing, or attaching radiation fins.

These mechanical external forces may cause package or chip cracking, or delamination at the boundary between the mold resin and the external pins which results in degraded moisture resistance.

5.3.1 Forming and Cutting External Leads

When mounting semiconductor devices onto printed substrates, care should be taken not to apply excessive force to the external leads when forming or cutting the external leads beforehand. (Fig. 5-26)

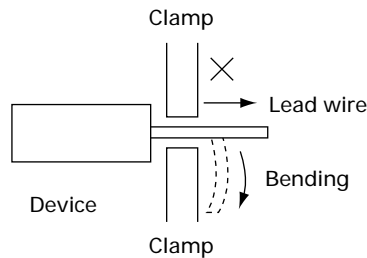


Fig. 5-26 Notes on Forming or Cutting External Leads

- (1) When bending external leads, clamp the external lead between the point at which the lead is to be bent and the package body. Do not bend external leads while holding the package body.
When using a metal mold, also do not apply stress to the package body.
Likewise, when cutting external leads, do not apply stress to the package body.
- (2) Do not repeatedly bend external leads.
- (3) Do not bend external leads in the thick direction of the lead.
- (4) Care should be taken as the external lead plating may be damaged depending on the bending method.

5.3.2 Mounting Devices on Printed Substrates

When mounting semiconductor devices on printed substrates, care must be taken not to apply excessive stress to the external leads. If the external leads bend or float, good solder contact with the printed substrate may not be obtained, resulting in a mounting defect. (Fig. 5-27)

- (1) The external lead attachment interval on the printed substrate should match the external lead interval of the device.
- (2) When inserting the device into the printed substrate, avoid forcibly inserting the device.
- (3) Leave an appropriate gap between the semiconductor device and the printed substrate.
- (4) When mounting a surface mounted type device on a printed substrate, if the external leads are deformed or float, good solder contact with the printed substrate may not be obtained, resulting in a mounting defect. Therefore, care must be taken not to deform the external leads.
- (5) When mounting semiconductor devices on printed substrates using mounting sockets, use an appropriate socket for each package.

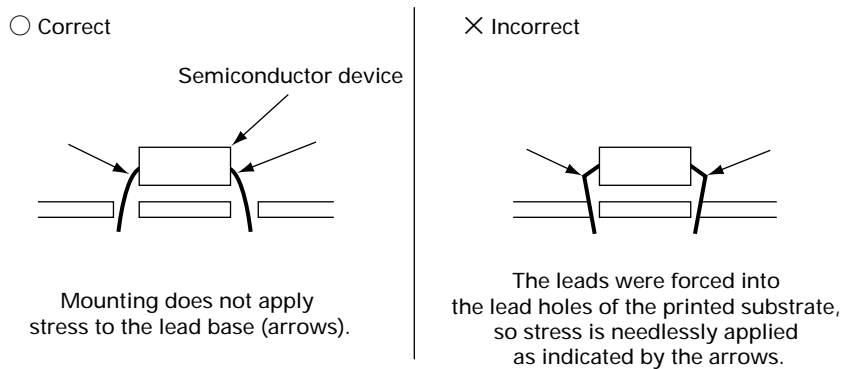


Fig. 5-27 Notes on Printed Substrate Mounting

5.3.3 Washing Methods

In principle, flux must be removed after soldering. Otherwise, flux residue may affect the reliability of components, printed substrate wiring or solder junctions.

- (1) Ultrasonic washing offers excellent washing effects in a short time, but care must be given to the applied frequency, output, washing time, and to avoid direct contact with the device and printed substrate in order to prevent device breakdown.
- (2) Do not rub marked surfaces during washing or while detergent has adhered to the device, as this may cause the marking to disappear. Care should also be taken as the marking may disappear if washing is performed for a long time.
- (3) Even when using solvents or washing just with water, washing should be performed so that sodium, chlorine and other reactive ions do not remain. Also, be sure to dry all parts thoroughly.
- (4) When using solvents, be sure to take into account public environmental standards and safety standards.

5.3.4 Attaching Radiation Fins

Care should be taken for the following points when attaching radiation fins to devices.

- (1) Use an appropriate attachment method so that excessive stress is not applied to the device.
- (2) Take care for flatness so that there is no burring or unevenness on radiator fins.
If radiator fins are inappropriate, sufficient radiation effects may not be obtained, or forced attachment may cause device characteristics degradation or mechanical breakdown.
- (3) When there are two or more radiator fin mounts, first lightly pre-tighten all of the mounts, then tighten to the prescribed torque.
- (4) Do not attach radiator fins to a semiconductor device after the device has been mounted on a substrate. Otherwise, excessive stress may be applied to the semiconductor device depending on the manner in which the device is mounted on the substrate. First attach the radiator fins to the semiconductor device, and then mount the device on the substrate.
- (5) Thermal conductivity is generally improved by coating the junction between radiator fins and semiconductor devices with silicon grease. In this case be sure to apply an even coat.

5.3.5 Handling of CCD Area Sensors and CCD Linear Sensors

(1) Handling during mounting (adhesion)

Remain within the following limits when applying a static load to packages during mounting or other work.

(Fig. 5-28)

- ① Compressive force: 39 N/face

(Do not apply any load 0.7 mm or more inside the outer perimeter of the glass surface.)

- ② Shearing stress: 29 N/face
- ③ Tensile force: 29 N/face
- ④ Twisting torque: 0.9 N·m

However, the following limits apply to area sensors with plastic packages. (Fig. 5-29)

- ① Compressive force: 50 N/face
- ② Twisting torque: 1.2 N·m

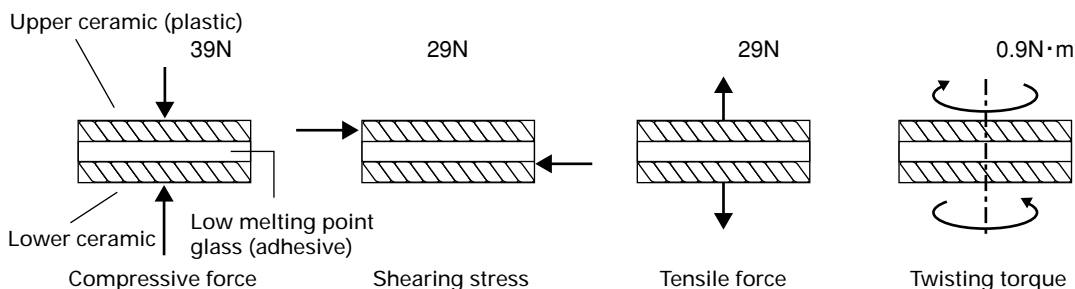


Fig. 5-28 Allowable Stress to Ceramic Packages

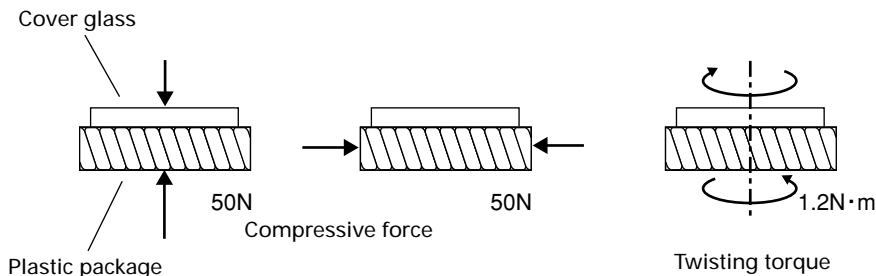


Fig. 5-29 Allowable Stress to Plastic Packages

If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for mounting, use either an elastic load, such as a spring plate, or an adhesive.

If the leads are bent repeatedly or metal, etc., strikes or rubs against the plastic package surface, the plastic may chip or fragment and generate dust.

In particular, the upper and lower ceramic (or the plastic and ceramic) of CERDIP packages and linear sensor plastic packages are adhered using low melting point glass (or adhesive). Care should be taken for these packages, as the following types of handling may cause the low melting point glass (or adhesive) to crack.

- (1) Applying a local load or mechanical shock to the low melting point glass (or adhesive) using tweezers or other pointed tool.
- (2) Twisting the upper and lower ceramic (or the plastic and ceramic) with the low melting point glass (or adhesive) as the fulcrum.

(2) Removing dust and dirt

The glass surfaces of elements must be kept constantly clean. Care should be taken not to either touch glass surfaces by hand or have any object come in contact with glass surfaces.

Dust or dirt adhering to glass surfaces should be removed by the following procedures.

- Dust or dirt adhered to glass surfaces
Blow off dust or dirt with an air blower. For dirt stuck through static electricity, ionized air is recommended.
 - Dirt or grease stains which cannot be removed by the above methods
Wipe away the dirt with a cotton bud moistened with ethyl alcohol in the order of ① and ② below.
- ① For the effective area and surrounding glass surfaces, incline the cotton bud (45° or less) and wipe away the dirt in the same direction as the lead arrangement as shown in Fig. 5-30.

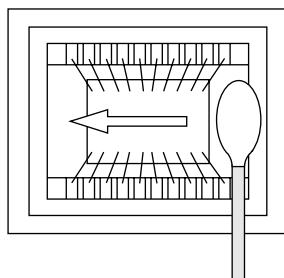


Fig. 5-30 Wiping the Glass Surface

- ② For the gap between the sealing glass and the package, hold the cotton bud straight up and wipe away the dirt as shown in Fig. 5-31.

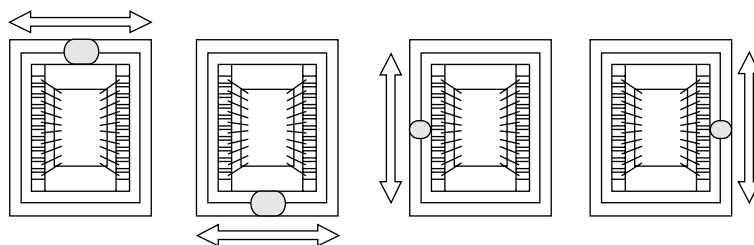


Fig. 5-31 Wiping the Sealing Glass Surface

[Notes]

- Do not wipe glass surfaces with a cotton bud if dust or dirt have not adhered.
- In step ①, do not allow the cotton bud to contact the glass edges or the ceramic surface.
- Do not reuse cotton buds.

(3) Handling of magazine-packed products

- Removing products

When removing products from magazines, remove the products by the following procedure to prevent lead bending due to dropping or other problems.

- ① Remove the rubber stopper. Be careful so that the products do not fall from the magazine at this time.
- ② Incline the magazine at approximately 30° over a conductive mat and let the products slide slowly out of the magazine. (Be careful as the products will fly out with great momentum if the magazine is inclined too much.)

Also, keep the magazine outlet at a height of 5 mm or less from the mat while removing the products. (Fig. 5-32)

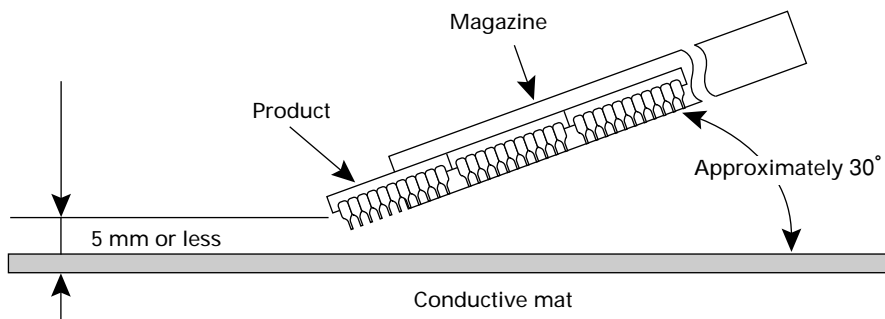


Fig. 5-32 Removing Products from Magazines

- Storing odd lots of products after opening magazines

After products have been removed, magazines may contain an odd lot of products. When storing these odd-lot magazines, inserting a rubber spacer of an appropriate length into the magazine and then fitting a rubber stopper is recommended to prevent the products from moving inside the magazine and being damaged by mechanical shocks, etc. (Fig. 5-33)

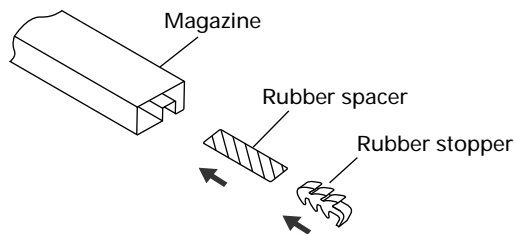


Fig. 5-33 Storing Odd Lots of Products in Magazines

5.4 Notes on Handling to Prevent Thermal Breakdown

Semiconductor devices have structures which combine a silicon chip, plastic encapsulating materials, copper and other metallic lead frames, and other materials, each of which have completely different thermal properties. In particular, when the plastic materials are exposed to high temperatures such as during soldering, the moisture accumulated in the plastic rapidly turns into steam and causes package cracking. The causes of delamination between the adhered portions of component materials, disconnection of conductors and other problems brought about by repeated heat stress are as follows.

- (1) The mechanical strength drops significantly at high temperatures.
- (2) Moisture in the air is absorbed and accumulated.

This section describes general precautions, particularly for product mounting, to prevent this type of thermal breakdown of devices.

5.4.1 Soldering

(1) Precautions during soldering

Semiconductor devices generally should not be left for long periods at high temperatures.

Even during soldering, regardless of whether hand soldering or reflow methods are used, if the soldering temperature is high and the soldering time is long, the device temperature may rise and result in degradation or breakdown. Therefore, soldering should be performed at the lowest temperature and shortest time possible.

(2) When soldering through hole device (THD) packages with a wave solder vat

This method dips the portions of the package lead pins to be soldered into the liquid surface of a jet solder bath. However, note the package may be damaged if the jet solder contacts the package body, so care should be taken not to allow the solder directly contact the package body.

In addition, when using a wave solder bath, the bottom of the substrate is heated by the solder heat, so substrate warping may occur due to the temperature difference between the top and bottom of the substrate.

If soldering is performed with the substrate in the warped condition, the substrate attempts to return to its original condition when it is taken from the solder bath, so excessive stress may be applied to the leads and package, causing solder junction cracking and lead and package damage.

Therefore, when using a wave solder bath, soldering should be performed in a manner that does not produce substrate warping.

5.4.2 Notes on Mounting Surface Mount Devices (SMD)

Substrate mounting methods for Surface Mount Devices (SMD) include infrared reflow, air reflow, and vapor phase reflow, etc. Thus, soldering methods which heat the entire package are often used.

In contrast to conventional THD where only the external lead pins are heated, the entire SMD package is suddenly exposed to high temperatures, so mold resin cracking and degraded moisture resistance must be taken into account as potential reliability problems.

In addition, SMD have short external lead pins, narrow pin intervals and large numbers of pins to facilitate high density mounting. Therefore, sufficient care must be taken when handling SMD.

General precautions when mounting SMD products are described below.

(1) Notes during mounting

When soldering is performed by infrared reflow or other methods which heat the entire device in the condition where the mold resin has absorbed moisture due to long-term storage in the normal environment or storage in a high humidity environment, the mold resin may crack or delamination may occur at the chip boundary.

Care should be taken for the following points during mounting.

- Set the soldering peak temperature as low as possible, and also reduce the number of processing times.
- Perform preheating to avoid subjecting devices to sudden temperature changes.
- Products which require moisture absorption control are packed in moisture-proof packing to avoid moisture absorption during transport and storage. To prevent the progression of moisture absorption after opening the moisture-proof packing, these products should be stored in the prescribed environment, and reflow mounting should be performed within the allowable storage time. If the mold resin has absorbed moisture, the devices should be baked before mounting.
- When removing mounted devices from printed substrates and then performing soldering again, use new devices if at all possible. If removed devices must be reused, take care for external lead deformation and also carry out baking before reusing devices which are susceptible to moisture absorption.
- When mounting devices on both sides of substrates, take care for the soldering temperature and time. In addition, moisture absorption must also be controlled during the first and second soldering periods for devices which are susceptible to moisture absorption.

(2) Deformation of external lead pins

If the external lead pins bend or float, good solder connection with the substrate may not be obtained, resulting in mounting defects. Particular care must be taken for the flatness of external leads so that pins do not float during mounting.

In addition, when mounting SMD, if strict control is performed for only the external lead pins and the substrate control is insufficient, good solder connection may not be obtained. Full care should be given to substrate warping and cream solder film thickness and uniformity, etc.

(3) Handling of taping parts

When using taping-packed SMD, static electricity is generated when the top cover tape is peeled from the carrier tape, and the SMD may become charged.

This charge voltage increases as the speed at which the top cover tape is peeled becomes faster.

High speed tape peeling and rubbing should be avoided as much as possible to prevent electrostatic breakdown.

(4) Other precautions

When coating SMD and other devices with plastic after mounting on a substrate, moisture absorption may cause the leak current to increase depending on the coating plastic, or the stress of the coating plastic may also produce mechanical stress on the plastic portions of devices. Therefore, post-coating reliability must be thoroughly confirmed when selecting the coating materials.

5.4.3 Reflow Mounting of SMD

SMD are mounted by applying a certain amount of solder paste to the printed substrate pattern using the screen printing or other method, and then placing the package on this solder paste. At this time the package is tentatively fixed by the surface tension of the solder paste. Then, when the solder is reflowed, the package leads and the printed substrate pattern are joined by the self-alignment effect due to the surface tension of the melted solder.

The types of reflow mounting are as follows according to the heating method. However, each heating method has its own characteristics, and the appropriate reflow method should be selected according to the characteristics of the mounting substrate and various mounted components to be soldered.

(1) Infrared reflow method

This soldering method irradiates infrared rays to the entire wiring substrate on which devices have been mounted. Multiple devices can be soldered at once, making this method suitable for mass production. However, it also has the disadvantage that if there is a large difference in device heights, temperature differences occur depending on the distance from the infrared ray source. There is also some equipment which uses both infrared rays and hot air.

(2) Hot air reflow method (Air reflow method)

This method heats air or inert gas with a heater, circulates this heated air or gas inside an oven, and performs solder reflow by thermal conduction from this hot air. Like vapor phase reflow, there is little temperature difference between the substrate and the device, and the temperature can be controlled to a certain temperature or less. Furthermore, solvent usage is not required, so cases of switching from vapor phase reflow to hot air reflow are increasing. However, the atmosphere allows solder oxidation to occur more easily than for vapor phase reflow, so it is more difficult to form solder balls, etc.

(3) Vapor phase reflow method

This method is also called vapor phase soldering (VPS). This method heats a solvent (fluorocarbon, etc.) with a vapor pressure of 200°C to 215°C to create a vapor layer, and reflows the solder inside this vapor layer. The use of solvent vapor facilitates temperature control, and there is no solder or flux sticking.

The VPS method is well suited for mass production and also has a high solderability level. However, the use of fluorocarbon-based solvents creates the problem of fluorocarbons in the exhaust, and with increased fluorocarbon regulations, many soldering facilities are being switched over to a different method.

(4) Laser heating method

This soldering method irradiates a laser beam at the soldered portions to melt the solder.

(5) Hot air heating method

This soldering method heats air, nitrogen or other gas with a heater and blows it from a nozzle. The thermal conductivity and heat capacity of the gas used as the heat medium are small, so a large gas flow must be supplied, making it difficult to ensure uniform and stable conditions. As a result, this method is not used much for mass production.

However, this method allows local melting of solder, so it is sometimes used to remove defective devices.

5.4.4 Recommended Conditions for Various SMD Mounting Methods

The mounting methods most generally performed for SMD are the infrared reflow method, vapor phase reflow method, and flow soldering method (wave soldering method). All of these mounting methods heat the entire package and apply strong heat stress to the package, so like the solder junction temperature, the package surface temperature must also be controlled from the viewpoint of maintaining reliability.

This section describes the recommended condition concepts using Fig. 5-34.

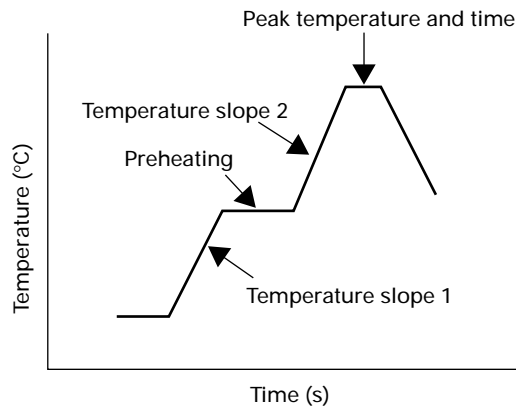


Fig. 5-34 Mounting Temperature Profile

(1) Temperature slope 1

When the temperature rises suddenly, the temperature at each part of the SMD package (for example, the package surface, interior, bottom) is uneven, and differences in the coefficients of thermal expansion of the materials may cause the package to warp and damage the chip. Therefore, care must be taken for the temperature rise rate slope.

(2) Preheating

The temperatures of the components, substrate and other parts are adjusted at the solder melting temperature or less to stabilize the solder junction and lessen the heat shock. The preheating temperature is generally set near the rated temperature for SMD.

(3) Temperature slope 2

Like (1) above, care must be taken for the temperature rise rate slope, and the peak temperature and time in (4) below must be kept within the prescribed limits.

(4) Peak temperature and time

The peak temperature and time require the most caution to minimize the damage sustained by the package. The peak temperature directly affects the drop in plastic strength (due to the resin temperature characteristics) and the steam pressure inside the package, so the temperature should be as low as possible. In addition, the steam pressure rises over time, so the soldering time must be as short as possible.

Fig. 5-35 shows the recommended conditions for infrared reflow and air reflow performed by the Sony Semiconductor Network Company.

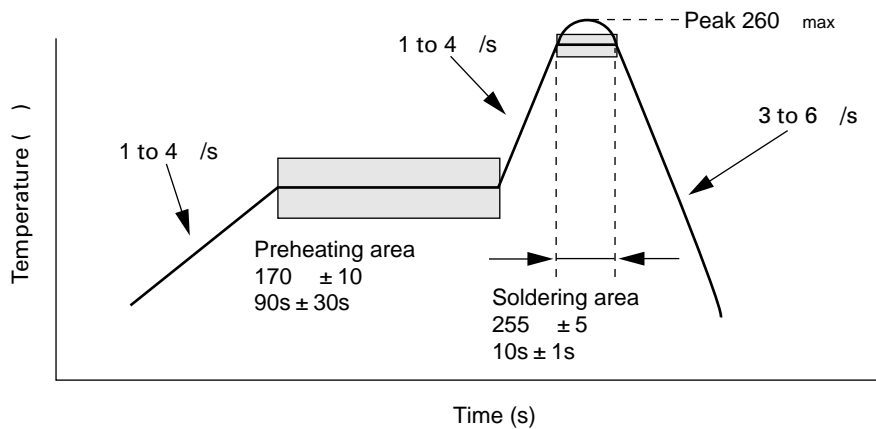


Fig. 5-35 Recommended Conditions for Infrared Reflow and Air Reflow

5.4.5 Soldering of CCD Area Sensors and CCD Linear Sensors

• Soldering

Care should be taken for the following points during soldering.

- (1) Do not let the package temperature exceed 80°C.
- (2) Absolutely do not use a mounting oven for soldering, as this may cause glass cracking or other problems.
- (3) Use a grounded 30 W soldering iron with a tip temperature of 350°C, and solder each pin in 2 s or less.

Solder should be applied to the areas shown in Fig. 5-36.

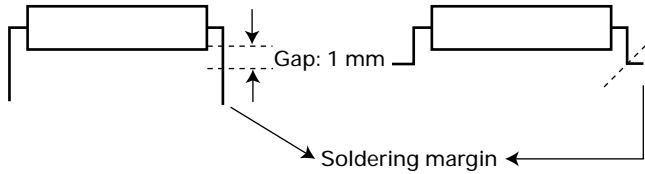


Fig. 5-36 Soldering Areas

- (4) Allow sufficient cooling when readjusting or removing CCD area or linear sensors.

In particular, the upper and lower ceramic (or the plastic and ceramic) of CERDIP packages and linear sensor plastic packages are adhered using low melting point glass.

If the temperature difference between point b (low melting point glass) and point a (lead base) in Figs. 5-37 and 5-38 is 100°C or more, the low melting point glass may crack.

Avoid local heating, rapid heating and rapid cooling

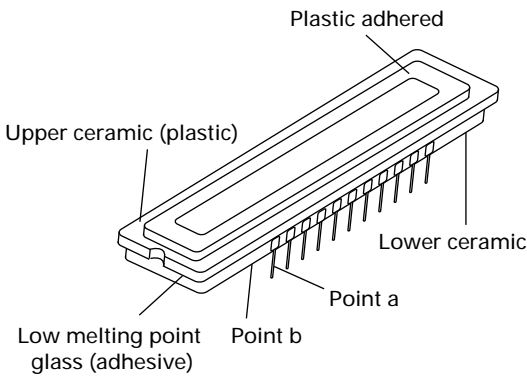


Fig. 5-37 Linear Sensor Structure

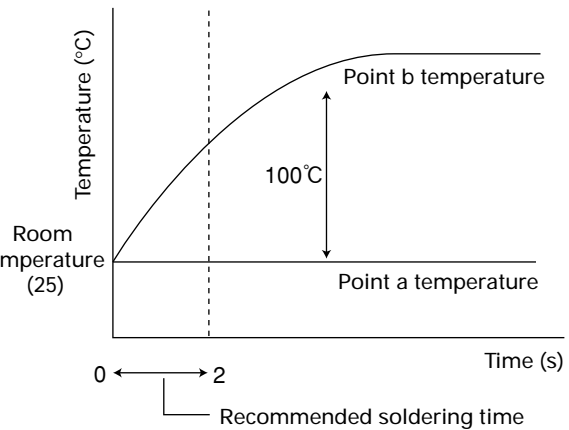


Fig. 5-38 Rise in Package Temperature due to Soldering

5.5 Notes on Handling to Prevent Misoperation

Unlike other semiconductor devices, microcomputers are semiconductors which first operate as completed products after having a program installed. Therefore, in addition to requiring the same care for handling as other semiconductors, it is also important to fully understand the microcomputer characteristics when creating programs in order to prevent accidents when products are used.

Hardware and software items which should be taken into account when using microcomputers are described below.

5.5.1 Notes on Hardware

(1) Power Supply

Power supply design must be thoroughly investigated in order to correctly operate not just microcomputers but all semiconductor products. Key points when designing power supplies include providing a stable voltage which satisfies the specifications, ensuring a current supply capacity that adequately satisfies the current consumption of the microcomputer (the current output from the microcomputer ports must also be taken into account), maintaining voltage for a certain time with respect to momentary voltage drops (this is related to the reset circuit described hereafter), blocking external noise to prevent it from affecting the microcomputer, and preventing noise generated by the microcomputer from leaking externally. Thus, it is not enough simply to produce voltage.

In terms of voltage stability, when the set uses an AC power supply or a battery, it is important to constantly maintain the voltage supplied to the microcomputer within the specified range with respect to the voltage fluctuations of this AC power supply or battery, and the microcomputer must also not be affected by sudden voltage fluctuations. It is particularly important to maintain voltage with respect to momentary power failures. However, a reset circuit must also be designed so that the set is reliably reset in the event of a power failure which might affect the microcomputer.

Insufficient current capacity may cause the supply voltage to drop with the result that the voltage falls below the range assured by the specifications. In addition to the current consumption prescribed by the specifications, the current flowing to the microcomputer also includes the current supplied from the output ports to external circuits, so this current changes according to the conditions under which the microcomputer is used. These elements must also be taken into account in the current capacity design.

When using an external power supply, noise may enter from that line. If this noise directly enters the microcomputer power supply, it may cause misoperation. Therefore, noise filters should be inserted to the external power supply input lines, or the power supply circuit should have low impedance. In addition, microcomputer operation may also be a source of noise, so noise countermeasures for power supplies are also important to prevent this noise from leaking externally.

There are also cases where separate power supplies for basic block circuits or for peripheral circuits such as an A/D converter are required in the microcomputer power supply pins. However, the required power supply characteristics differ in many of these cases. Power supplies must be connected to all of these pins, but it is important to check the specifications listed in the product data sheets and to design power supplies which satisfy the requirements.

(2) Oscillation Circuit

Oscillation circuits are important circuits which generate the microcomputer operating clocks, so oscillation must be stable and uninterrupted under the hypothesized operating conditions. Elements which can be used for oscillation include crystal oscillators and ceramic vibrators, but the added capacitance and other constants must be optimally set for each of these to ensure that oscillation starts reliably and to maintain stable oscillation. Furthermore, the operating voltage range also affects the circuit constant settings. The optimum added capacitance under these conditions must be determined using the final set board, and a reliable method for achieving this is to provide the board and intended microcomputer to the oscillator manufacturer and have the oscillator manufacturer measure the optimum capacitance.

(3) Reset Circuit

Like the power supply and oscillation circuits, the reset circuit is also an important circuit for reliably operating microcomputers. The circuit structure must reliably apply a reset not only during power-on, but also when momentary voltage drops occur.

During power-on from the zero-voltage state, a reset is applied even with a simple CR delay circuit. However, this cannot support cases where the voltage drops momentarily such as momentary power failures, and reliably applying a reset when the voltage drops gradually and the supply voltage is at the specification or less is also difficult, which can lead to malfunction.

When designing the reset circuit, the power-on reset cancel voltage, reset application time, and the voltage setting at which reset is applied when the voltage drops should all satisfy the product specifications. In addition, the circuit must also be able to reliably apply a reset when momentary voltage drops occur.

(4) Test Mode

Microcomputers switch between normal operation and test mode according to the input level of a certain pin during reset in order to make the test mode settings. The test pins also function as general-purpose ports to maximize the valid pins, and can be set to the level for entering test mode by an externally connected circuit. These pins are noted in the User's Manual of each microcomputer, and these contents should be fully understood before designing circuits.

(5) Noise Countermeasures

Thorough noise countermeasures must be taken for both external influences on microcomputers and the external influence of microcomputers. Although mentioned under Power Supply, the processing for each pin is also described here. In addition to power supply pins, input/output pins are also susceptible to the effects of noise. These pins are each connected to external circuits, so countermeasures suited to these circuits are required. Simple CR filters are generally used, but when directly controlling signals outside the substrate on which the microcomputer is mounted, the circuit configuration should connect through a buffer circuit to prevent noise received by long wiring paths from reaching the microcomputer.

Noise emitted by microcomputers must be suppressed by external circuits, and this requires optimization of the power supply and signal line layouts. Attaching the above CR filter to each pin is also effective in this case. There are often substrate design limitations, but it is important to first determine how to implement noise countermeasures, and then proceed with the overall substrate layout.

5.5.2 Notes on Software

(1) Initial Value Settings

When reset is canceled, operation starts in accordance with the program built into the microcomputer. However, initial settings must be made in the initial stages of this program to enable the various built-in functions. The initial RAM status is undetermined, so the areas to be used must all be set initially by the program. The initial register values of various peripheral circuits may be undetermined after reset, so initial values must be set for these as well. The initial register status for each peripheral circuit is noted in the User's Manual, so these must all be checked and set.

(2) Deadlock

When compiling a program, the program may wait for a certain phenomenon to occur before shifting to the next process. In this case, if the anticipated phenomenon does not occur for whatever reason, the program cannot shift to the next process, and the current process is repeated endlessly, making it appear as if operation has stopped. This is called deadlock, and countermeasures for avoiding deadlock must be considered. In addition to the anticipated phenomenon, timer interrupts and other regularly occurring phenomenon are also generally checked at the same time, so if the anticipated phenomenon does not occur for a certain time or more, this is processed as an error and the corresponding countermeasure routine is executed. This makes it possible to know the cause when operation stops, and is useful for investigating causes when trouble occurs.

5.6 Notes on Product Specifications, Packing, Transport and Storage

5.6.1 Notes on the Use of Semiconductor Devices

The Sony Semiconductor Network Company makes the utmost efforts to improve quality and reliability, but due to the nature of semiconductor devices, a certain percentage of devices may malfunction or fail. When using semiconductor products manufactured by the Sony Semiconductor Network Company, customers are requested and responsible for ensuring safe equipment and system designs to prevent accidents resulting in death, injury or damage to property from occurring as a result of semiconductor failure.

Note that when designing equipment and systems, the latest product specifications should be checked, and products should be used within the assured ranges.

Semiconductor products listed in catalogs and sold assume use in general electronic equipment (home appliances, telecommunications equipment, measuring instruments, office equipment, etc.). Customers should be sure to consult their Sony sales representative beforehand when planning use for applications requiring special quality and reliability, or in equipment and systems (automobiles, traffic equipment, medical equipment including life-support devices, safety devices, aerospace equipment, nuclear power control equipment, etc.) where product failure or malfunction may pose a direct life- or injury-threatening risk or damage to property.

Special consideration and selection is required for products which demand high reliability.

5.6.2 Maximum Ratings (Absolute Maximum Ratings)

The maximum ratings of semiconductor devices are normally prescribed by the [Absolute Maximum Ratings]. According to JIS C 7032, absolute maximum ratings are prescribed as "Limit values which must not be exceeded even momentarily, or limit values for which the values of two or more items must not be reached simultaneously when specification values are established for two or more items." Exceeding absolute maximum

ratings even temporarily causes degradation or failure, and even if the product continues to operate for some time thereafter, the life is significantly shortened. Therefore, when designing electronic circuits using semiconductor devices, care must be taken not to exceed the maximum ratings of these devices even due to fluctuations caused by external conditions during operation.

5.6.2.1 IC Maximum Ratings

Maximum ratings indicate the operating limit values for that IC, and parameters such as those shown in Table 5-8 are generally prescribed. When actually using ICs, operation must stay within these prescribed ranges.

Table 5-8 Examples of Absolute Maximum Ratings

Item	Conditions	Rating value	Contents
Supply voltage (V _{DD}) (V _{CC})	T _a =25°C Measured relative to the V _{SS} pin	7.0 V (for a 5.0 V device)	This is the maximum voltage that can be applied between the power supply pins and the GND pins. 1. This is related to the endurance voltage of the transistors inside the IC, and breakdown may occur if this voltage is exceeded. 2. CMOS devices may break down due to dynamic latch-up or the injection of large quantities of hot carriers.
Input and output voltages (V _{IN}) (V _{OUT})	T _a =25°C Measured relative to the V _{SS} pin	-1.0~7.0V	This is the maximum voltage that can be applied between the input/output pins and the GND pins. This voltage generally cannot be larger than the supply voltage. 1. Parasitic elements configured on the input and output pins may experience endurance voltage-related breakdown. 2. Breakdown may be caused by latch-up triggered by the input or output pins.
Allowable power dissipation (P _D)	T _a =25°C	1W	This is the maximum power consumption allowed inside the IC. 1. Breakdown may be caused by internal heat generation during operation. 2. This value differs according to the degree of IC integration and the heat radiation characteristics of the package.
Storage temperature (T _{stg})	-55~150°C		This is the allowable ambient temperature range during storage. 1. The temperature is limited by the package materials and the intrinsic properties of semiconductors.
Junction temperature (T _j)			This is the maximum allowable junction temperature value at which continuous operation is possible.
Operating temperature (T _{opr})	0~70°C		Recommended operating temperature condition range: IC operation and functions can be assured within this temperature range, but the electrical characteristics indicated at T _a = 25°C cannot necessarily be assured.

Note) Rating values are prescribed by the individual specifications for each device.

Fig. 5-39 shows the relationship between various IC maximum ratings.

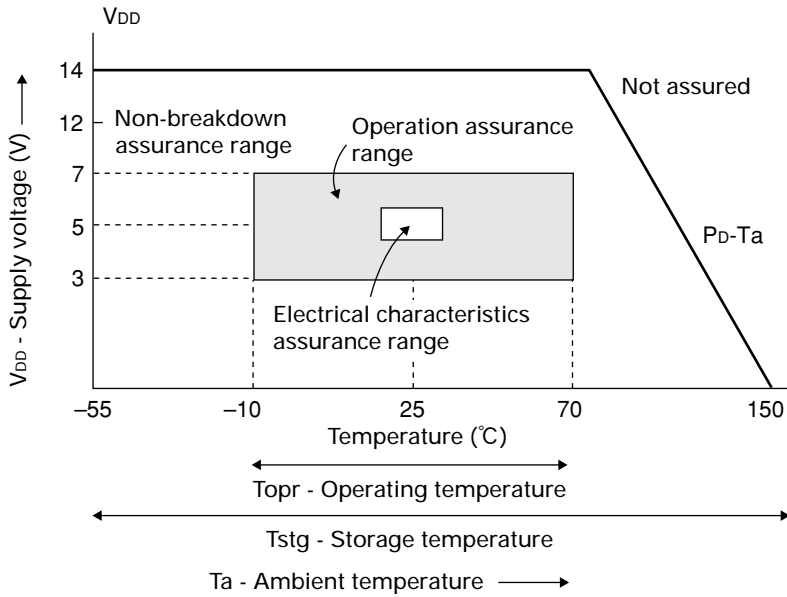


Fig. 5-39 Relationship between Various Maximum Ratings

IC maximum ratings are assured continuously, but the following guidelines should be taken into account, particularly for power ICs.

- Average current: $ICC \times 0.5$
- Peak current: $ICC \text{ (peak)} \times 0.8$
- Average power: $\text{Maximum rating} \times 0.5$

5.6.2.2 Derating of Diodes, Transistors and Power Devices

With respect to excessive conditions, the peak voltage, current, power and junction temperature including surge and other factors are generally set to the maximum ratings or less, and derating for reliability design is performed using the average values. (Table 5-9)

Derating: Intentionally reducing loads from rating values to improve reliability. (JIS Z8115-1981)

Table 5-9 Derating Design References

Derating element		Diode	Transistor	Power device
Junction temperature	T _j	Maximum rating ×0.7 times or less	Maximum rating ×0.7 times or less	Maximum rating ×0.7 times or less
		Power consumption, ambient temperature and radiation conditions $T_j = P_D \times \theta_{j-a} + T_a$		
Voltage	V _{CBO} , V _{CEO}	Maximum rating ×0.8 times or less	Maximum rating ×0.8 times or less	Maximum rating ×0.8 times or less
Current	I _c , I _B , I _E	I _F , I _Z ×0.7 times or less	Maximum rating ×0.8 times or less	Maximum rating ×0.8 times or less
	I _c (peak)	Maximum rating or less	Maximum rating or less	Maximum rating or less
Power	P _c , P _D	According to the derating curve within the T _j range		

5.6.3 Notes on Packing, Transport and Storage

5.6.3.1 Packing Methods

In order to maintain the high quality and high reliability of semiconductor devices (hereafter “devices”) the following three packing methods are mainly used in accordance with the package shape and mounting format.

- | | |
|---------------------|--|
| (1) Magazine | THD packages (DIP, SDIP, SIP) and SMD packages (SOP, SSOP, etc.) |
| (2) Tray | SMD packages (QFP, LQFP, SOP, SSOP, etc.) |
| (3) Embossed taping | SMD packages (QFP, LQFP, SOP, SSOP, etc.) |

Care should be taken for electrostatic breakdown during handling, package cracking during mounting due to package moisture absorption, mechanical breakdown due to shocks, lead bending, and other causes of device breakdown.

(1) Magazine packing

- The magazine, stopper pin and rubber plug materials are PVC plastic. (Fig. 5-40)
The surfaces are coated with an anti-charging agent to prevent static electricity. Care should be taken as this anti-charging agent is water soluble, and the effects will be lost if the magazine is dampened by water or stored in a high temperature and high humidity location. Apply the anti-charging agent again when reusing magazines.
- The magazines and stoppers do not have heat resistant specifications. (70°C max.)
When baking (drying at high temperature) is necessary, transfer the devices to a metal magazine. At this time, care must be taken to prevent lead bending particularly for SMD, such as by using a transfer jig.
- Magazines are packed in aluminum laminate moisture-proof bags to prevent moisture absorption and block contact with the outside air, and devices should be mounted as soon as possible after opening this packing. In addition, confirming the solderability is recommended before using products that have been stored for long periods.

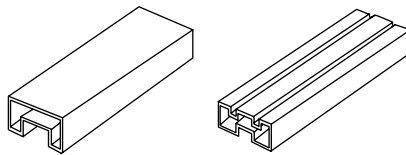


Fig. 5-40 Conductive Magazines (Tubes)

(2) Tray packing

Trays come in heat resistant specifications and normal temperature specifications. (Fig. 5-41) When products in normal temperature specification trays are to be baked (dried at high temperature), these products must be transferred to a heat resistant specification tray.

There are two types of trays as follows according to the molding method.

1. Injection molded hard trays
2. Vacuum molded soft trays

The plastic used for injection molding is mixed with carbon to prevent charging, and is conductive. Anti-charging materials are mixed into vacuum molding materials or applied in a coat over the plastic sheet, so both types have anti-charging specifications.

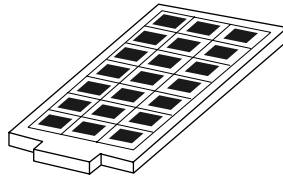


Fig. 5-41 Tray

Tray products are mainly QFP, LQFP, BGA and TSSOP package products which are stored and shipped in injection molded hard trays, and CCD, LCD and laser diodes which are stored and shipped in vacuum molded soft trays.

(3) Embossed taping packing

To improve mounting efficiency during set assembly, semiconductor products are stored in embossed conductive plastic tape, wound onto reels, and shipped in aluminum laminate bags with desiccants and humidity indicators. Embossed taping storage standards are prescribed by EIA 481A and JIS C 0806, and the widths of 8, 12, 16, 24, 32, 44 or 56 mm are used according to the product size. (Fig. 5-42)

For details, see the individual product specifications.

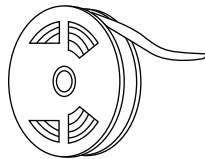


Fig. 5-42 Taping

The tape and reels do not have heat resistant specifications, so baking is not possible. When a reel is only partially used during mounting, care must be taken for handling to prevent moisture absorption by removing the reel from the moulder and repacking it in the original bag, etc.

The carrier tape and top cover tape are heat sealed with adhesive, and the peeling strength prescribed by EIA is assured for a period of one year after shipment.

5.6.3.2 Packing

Devices contained in magazines, trays and embossed taping are stored and shipped in inner and outer boxes to avoid the effects of external shocks during transport, rain water during storage, or contamination from the outside air, etc.

(1) Outer carton

- Products are stored and shipped in cardboard outer cartons to minimize the effects of shocks, vibration, humidity and other factors on devices.
- Cardboard and other outer cartons have symbol marks urging caution during handling such as those shown in Fig. 5-43 for “Avoid static charges”, “Fragile”, “Keep dry” and “This side up”. The caution marks should be observed during storage and transport.

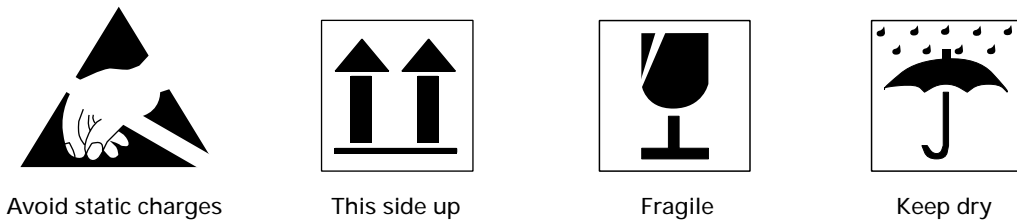


Fig. 5-43 Packing Carton Markings

(2) Inner Carton

- Magazine packing (see item 5.6.3.1) is used for THD, SOP and other packages with the external lead pins in two directions. The Sony Semiconductor Network Company places SMD packages and S-Pd PPF products in moisture-proof packing bags and then stores these bags in an inner carton.
- Moisture absorption affects Surface Mount Device (SMD) quality, and moisture-proof packing aims to prevent moisture absorption during storage. Devices, desiccants and moisture indicators for detecting humidity are placed in aluminum laminate bags which are deaerated and heat sealed to block outside air and prevent the entry of moisture. (Fig. 5-44)
After the bags are opened, control should be performed so that devices are used within the specified time.

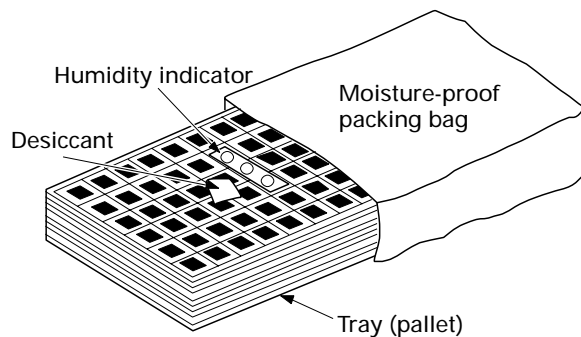


Fig. 5-44 Moisture-proof Packing

- Taping is used for SMD due to advantages such as easy handling during automatic mounting and high packing density. Note that the tape and reel do not have heat resistant specifications, so baking is not possible. The carrier tape and top cover tape peeling force (Fig. 5-45) is 0.1 to 0.7 N for a peeling speed of 300 mm/min and a peeling angle of 165° to 180° with respect to the adhered tape surface. The peeling strength is assured for a period of one year after shipment.

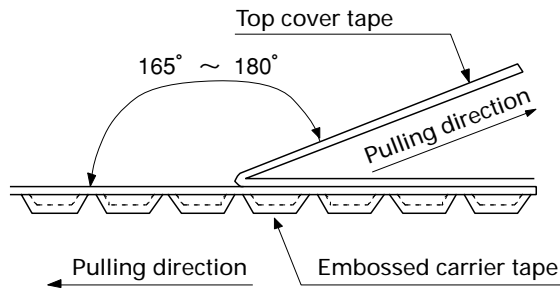


Fig. 5-45 Tape Carrier Peeling Method

[Note]

When the humidity indicated by the humidity indicators of devices in moisture-proof packing exceeds 30% (pink), these devices must be dried again (baking at 125°C for 24 h or 125°C for 48h).

5.6.3.3 Transport Methods

If handling is rough and strong shocks are applied during transport, Surface Mount Devices (SMD) in particular may experience lead bending, causing the coplanarity of the external leads to worsen (80 μm or more) and resulting in trouble during soldering. Also, if the aluminum laminate moisture-proof packing bags become torn, moisture is absorbed from the outside air and may cause package cracking.

The contents of caution marks on packing cartons are as follows.

- Fragile
If packing cartons are thrown or dropped during handling, the packing materials and possibly the devices themselves may be damaged. Semiconductor devices should be handled as “fragile” items.
- This side up
Packing cartons should be placed facing the correct direction as indicated on the packing carton during transport. If packing cartons are turned upside down or on their sides, unnatural force may be applied to and damage devices.
- Keep dry
When cartons absorb water, the strength drops drastically, so cartons must not be allowed to become wet especially during transport in rain or snow.
- Avoid static charges
This is not a caution during transport, but is indicated as a caution during set mounting.

In addition to the above cautions, devices must be transported in a manner which minimizes mechanical vibrations and shocks as much as possible.

5.6.3.4 Storage Methods

(1) Storage of assembled products

- Storage environment temperature

Assembled products should be stored indoors under ambient conditions of 0°C to 35°C and humidity of 85% or less. The so-called normal temperature and humidity are suitable for the temperature and humidity of locations where semiconductor devices are stored.

- Storage time limit

The limit for non-taping products (products packed in magazines and trays) is 1.5 years from the week indicated by the marking. The limit for taping products is the shorter of one year from the taping package label issue date or 1.5 years from the week indicated by the marking.

- Ambient conditions

Avoid storage in locations exposed to direct sunlight, locations where corrosive gases are generated, or dusty locations.

- Magazines and non-heat resistant trays may deform if exposed to direct sunlight.

- Corrosive gases cause the external lead pins or metal casings of devices to corrode (deteriorated solderability).

- Temperature changes (avoiding condensation)

Moisture condenses on packed products in locations where the temperature changes suddenly. Semiconductor devices must be stored in locations where the temperature changes as little as possible.

- Load limits

Avoid stacking or placing heavy objects on packing boxes as much as possible to avoid applying loads to devices.

The maximum mass of the outer box is prescribed as 10 kg.

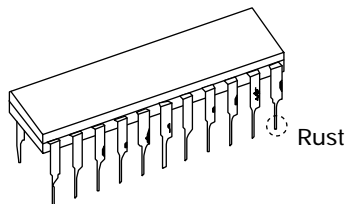
- The storage location should not be exposed to radiation, strong electromagnetic fields or static electricity.

(2) Long-term storage

When storing devices for long periods, the storage time limit shall be 5 years or less based on the product packing specifications and under storage environment conditions of temperature 30°C and humidity 85% or less. However, storage in the taping condition is prohibited.

Devices are stored in the loose condition (packed in trays or magazines), taping work is performed if necessary, and devices are shipped as quickly as possible.

Special care must be taken as follows for long-term storage, as the lead pin solderability may deteriorate, the lead pins may rust (Fig. 5-46), or the electrical characteristics may deteriorate.



When stored for long periods, the lead pin solderability may deteriorate.

Fig. 5-46 Lead Rusting

- Packing

When long-term storage (one year or more) is anticipated from the start for THD (DIP, SIP, etc.) products without moisture-proof packing, these products should be placed in moisture-proof packing or other countermeasures should be taken to prevent deteriorated solderability and rust.

- Check items

When a long time (one year or more) has passed in the stored condition, the solderability and lead rusting should be inspected prior to use. The electrical characteristics should also be inspected as necessary.

(3) Handling of products in moisture-proof packing

As packages become thinner, package cracking in soldering processes which use methods that heat the entire package (dip, reflow) has become a problem. Package cracking occurs when package resin that has absorbed moisture from the air is exposed to a high temperature atmosphere during soldering, and it is necessary to suppress moisture absorption as a countermeasure.

Resin basically has a nature which easily absorbs moisture, so it easily takes in moisture from the air. For this reason, Sony uses moisture-proof packing to prevent SMD from absorbing moisture. However, it should be kept in mind that moisture absorption starts when the moisture-proof packing is opened.

- Opening moisture-proof packing

Moisture-proof packing must absolutely not be opened except when not using all of the SMD contained in that packing. Also, care should be taken during all work to prevent holes from being opened in the aluminum laminate bags. If holes are opened, devices must be transferred to a new aluminum laminate bag which is then deaerated and heat sealed.

When storage in the opened condition is unavoidable, use a SMD stoker controlled to a humidity of 30% or less.

- After opening moisture-proof packing, devices should be used according to the package mounting rank instructions. If moisture absorption progresses, baking (125°C for 24 h) is required.
- When temporary storage is required after opening moisture-proof packing, place the devices together with a desiccant inside an aluminum laminate bag, fold the opening two or more times, and seal it with a clip or cellophane tape as shown in Fig. 5-47 to suppress moisture absorption.
- Taping packed products cannot be baked.

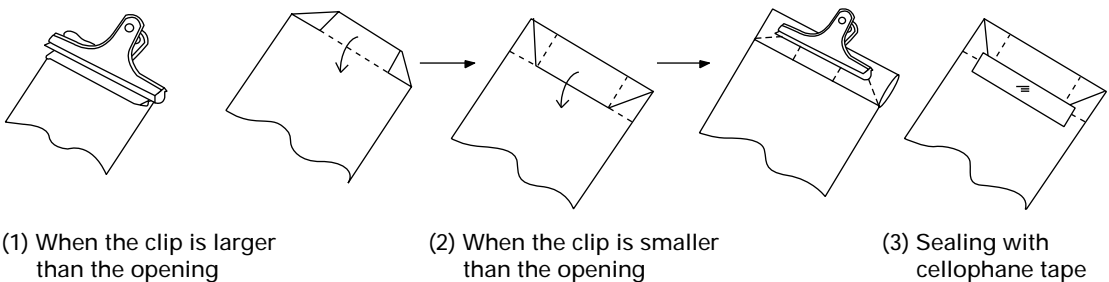


Fig. 5-47 Moisture Absorption Measures after Opening

5.6.3.5 Reusing Packing Materials

The Sony Semiconductor Network Company makes active efforts to recover and reuse packing materials such as magazines, trays, reels and some cardboard boxes in order to reduce plastic waste as much as possible. Cooperation with the collection of used packing materials is requested to protect the environment. Please contact your Sony sales representative for details.

5.6.4 Handling LCDs

(1) Electrostatic countermeasures

TFT-LCD panels are easily damaged by static charges, so be sure to take the following protective measures.

- a) Use non-chargeable gloves, or simply use bare hands.
- b) Use a wrist strap when directly handling panels.
- c) Do not touch any electrodes of a panel.
- d) Wear non-chargeable clothes and conductive shoes.
- e) Install conductive mats on the work floor and worktable.
- f) Keep panels away from any charged materials.
- g) Use ionized air to discharge the panels when handling.

(2) Dust and dirt countermeasures

- a) Operate in a clean environment.
- b) When delivered, the panel surface (glass) is covered by a protective sheet. Take appropriate measures to prevent static charges, and then peel off the protective sheet carefully so as not to damage the glass surface.
- c) Do not touch the glass surface, as the surface is easily scratched. When cleaning is required, gently wipe the glass surface with a clean-room wiper moistened with isopropyl alcohol. Be careful not to leave a stain on the surface.
- d) Use ionized air to blow dust off the glass surface.

(3) Other handling precautions

- a) Do not twist or bend flexible print circuits especially at the connecting region because they are easily deformed.
- b) Do not drop panels.
- c) Do not twist or bend panels or panel frames.
- d) Keep panels away from heat sources.
- e) Do not dampen panels with water or other solvents.
- f) Avoid storing or using panels at a high temperature or high humidity, as this may adversely affect the panel characteristics.
- g) The minimum bending radius of flexible print circuits is 1 mm.
- h) When mounting panels, use a screw tightening torque of 3 kg·cm or less.
- i) Use filters as appropriate to protect panels.
- j) Do not apply pressure to panel locations (cover, etc.) other than the mounting holes.