CHAPTER 3 - FAILURE ANALYSIS

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3.1 What is Failure Analysis?

Failure analysis consists of confirming reported failures and clarifying failure modes or mechanisms using electrical measurements and various scientific analysis technologies.

This chapter introduces specific failure analysis methods. However, before performing the actual analysis work it is necessary to thoroughly investigate failure circumstances and accurately understand the failure contents. This makes it possible to determine the optimum analysis methods and carry out swift processing.

Fig. 3-1 shows an example failure analysis procedure.

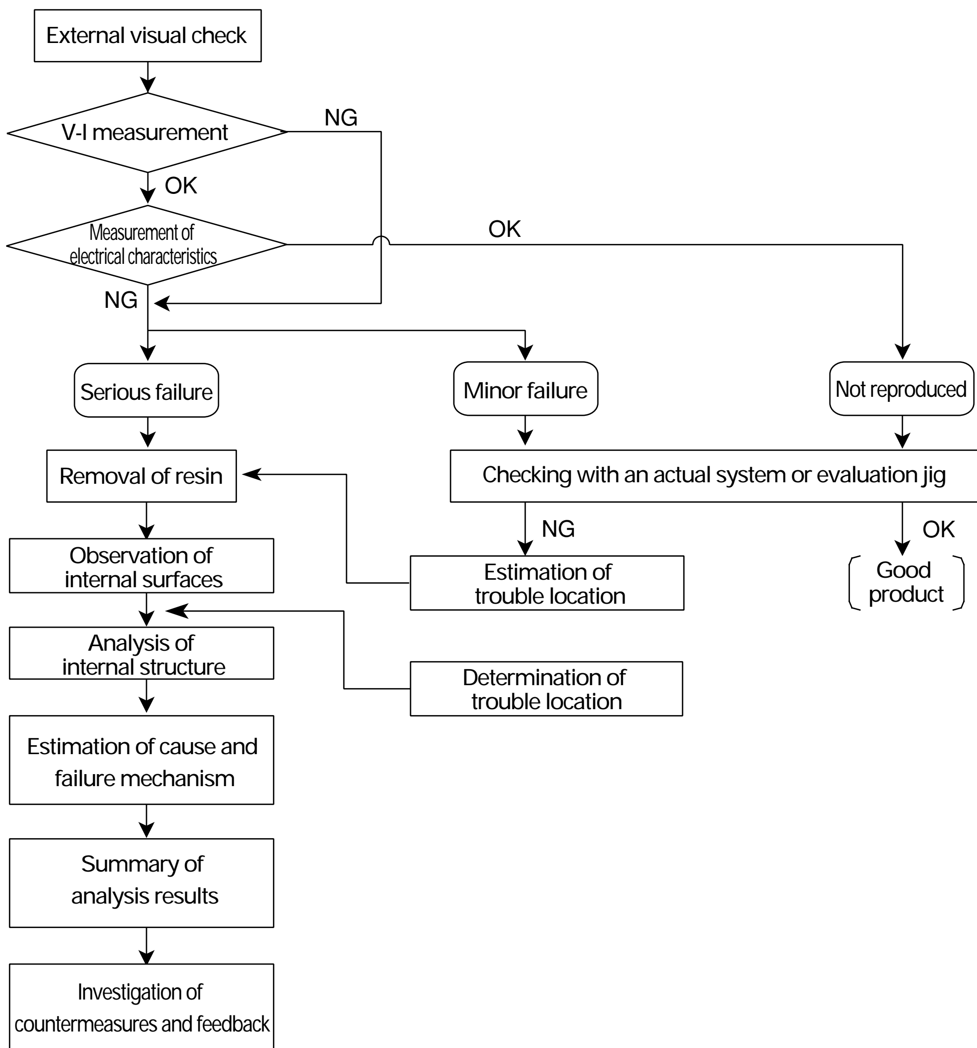


Fig. 3-1 Failure Analysis Procedure

3.2 Necessity of Failure Analysis

As semiconductor devices become more highly integrated and incorporate more advanced functions, manufacturing processes are becoming more miniaturized and complex, and include diverse reliability factors. In addition, semiconductor devices have come to be used over an extremely wide range of fields, so failure causes and mechanisms are also complex.

Under these circumstances, an extremely high reliability level is required of semiconductor devices.

Reliability must be built in from the device development stage to the manufacturing stage in order to ensure a high level of reliability. Therefore, it is important to analyze failed products occurring in reliability tests, customer processes and the market, clarify failure modes and mechanisms, and provide feedback to improve the manufacturing and design processes.

Failure analysis is not simply investigating the failure causes and mechanisms of failed products. It is a vital and essential technical field for the design and manufacture of high quality and high reliability devices.

3.3 Failure Analysis

3.3.1 Investigation of Failure Circumstances

When failures occur, it is important to understand the failure circumstances in order to determine the failure analysis methods and procedures so that failure analysis can proceed smoothly.

When a failure sample is obtained, as much information as possible about that sample is gathered at the same time. The product name, production lot number, number of failures and failure rate, trouble contents, mounting conditions, place where the trouble occurred, circuits used, operating conditions, environmental conditions and other information are understood accurately and compiled into a list to assist in estimation of the failure mechanism and simulations, etc.

3.3.2 Handling of Failure Samples

Failure samples contain a great deal of information, and are highly valuable as their number is limited. If failure analysis is unsuccessful it is possible that no information may be obtained. Therefore, the following precautions should be observed when handling failure samples.

(1) Maintenance of failure conditions

If stress (mechanical, electrical, thermal) which changes the failure conditions is applied prior to analysis, accurate analysis is impossible.

Therefore, failure samples must be processed and stored in a manner which maintains the failure conditions.

(2) Lead processing

When analyzing devices which are solder-mounted onto substrates, samples removed from substrates may require lead processing for LSI tester measurement or other analysis. The utmost care should be taken during this processing not to apply heat to the device or to damage the leads.

(3) Storage

In addition to the identification of samples, care must also be taken for storage.

Care must be taken for environmental factors such as temperature and humidity, and also to prevent the progression of electrical and mechanical damage. Care must also be taken for storage to prevent the adherence of dust or surface scratching of samples with decapped packages.

3.3.3 External Visual Inspection of the Package

Visual inspection of the external condition is important, and in many cases provides useful information for analysis when quality trouble occurs.

The entire package should be carefully observed using the naked eye to ascertain differences from good products, and then detailed observation should be made using a stereoscopic microscope. With the stereoscopic microscope, it is important to adjust the lighting in a variety of angles to obtain the best view of the observed location. If necessary, abnormal locations should also be searched for using an optical microscope with higher magnification (approximately 100 to 1000×). If further detailed observation is required, SEM is used to search for break surfaces, discoloration and migration, and SAT is used for internal analysis such as delamination and cracking. When elemental analysis is required and a sufficiently large number of samples is available, atomic absorption spectrometry or other methods are used. When taking samples of foreign matter from minute areas is difficult, electron probe micro analysis (EPMA) is used.

Key points for external visual inspection are as follows.

(1) Voids and pinholes

The mold resin normally used for semiconductor devices has low viscosity and is molded at low pressure, so residual air bubbles may cause voids and pinholes. (Void: air bubble inside the package, pinhole: air bubble on the package surface) When voids occur on element surfaces or over metal wiring, water may condense and corrode the wiring, causing problems with moisture resistance reliability.

In addition, pinholes are appearance and reliability defects, and cracking may originate at pinholes (and voids) during reflow. The generation of voids and pinholes is greatly influenced by the water content, viscosity and gap ratio (materials and mold structure) of the mold materials. These factors can be suppressed to a level which poses no problems for practical use by setting appropriate conditions.

(2) Package cracking

Cracking is caused by the penetration of moisture from outside the package. Cracking may be easily overlooked depending on the package structure and materials, so sufficient care must be taken for observation. Inspection using fluorescent penetrant fluid is effective for observing minute cracks.

(3) Mechanical damage to external pins

Damage modes differ depending on the pin shape, load, environment and other factors.

These modes include fatigue damage caused by repeat stress, shock damage caused by sudden stress, and creep damage caused by application of a constant stress over a long time. Wave-like patterns appearing on crack and break surfaces indicate that these are due to mechanical fatigue. For example, a dish-shaped or ratchet-shaped break surface indicates that there exists stress concentration at that point.

(4) Adherence of foreign matter

Foreign matter adhering to external pins is a cause of connection defects when mounting on a substrate.

This problem occurs when the handling or work environment in the manufacturing process or the storage environment is inappropriate. In addition, conductive foreign matter (such as whisker-like plating formations) occurring between external pins may cause short circuits between leads.

(5) Contamination

Contamination by remaining traces of water, oils, flux, and various spray liquids (such as insulation materials) may cause connection and/or leakage defects.

(6) Lead discoloration

To improve solderability and resistance to corrosion of the lead frames used in semiconductor devices, the external leads are normally solder-plated except for S-Pd PPF (Sony Specification palladium Pre-Plated lead Frame). Plating discoloration is caused by chemical reactions such as oxidation and sulfurization due to heating, flaws in the base material, incomplete pretreatment, and plating flaws, etc.

(7) Metal migration

When voltage is applied at high temperatures and high humidity, metallic ions inside the insulation material or at its surface migrate from the positive electrode to the negative electrode where they collect, are reduced and precipitate. This may ultimately lead to a short between the two electrodes. Inspection using a metallurgical microscope or EPMA is effective for observing these features.

(8) Stress corrosion cracking of leads

Stress corrosion cracking occurs when Cu-Zn alloys and other copper based alloys which are subject to tensile stress due to external stress or internal residual stress are exposed to ammonia, amines, high temperatures and humidity or other environmental factors. These conditions can be judged by inspecting cracking break surfaces and observing grain boundary conditions and other factors using SEM.

3.3.4 Evaluation of Electrical Characteristics

(1) Evaluation using a LSI tester

Test programs for design evaluation and analysis are used to evaluate the electrical characteristics of failure samples.

These results are then used to classify and analyze failure modes, infer failure mechanisms, and determine subsequent analysis methods.

Evaluation of electrical characteristics makes it possible to accurately understand failure mechanisms in detail from the failure circumstances, and effective analysis methods can be determined based on these results.

In addition, when evaluating memory LSI the detailed failure location can often be pinpointed on the chip, so detailed evaluation of the electrical characteristics is important.

(2) DC characteristics evaluation

This evaluation method investigates the DC characteristics of chips using a curve tracer, picoammeter and other equipment.

Pin damage, open connections, short circuits, DC characteristics deterioration and other problems can be detected.

The analysis sensitivity for minute deterioration and damage can be improved by comparing the characteristics with good chips to ascertain the difference.

(3) Mounting evaluation

This method mounts the sample on actual electronic equipment for evaluation.

This method is effective for reproducing and confirming failure modes when failure locations cannot be determined using methods (1) and (2) above. When the failure cannot be determined using methods (1) and (2) but is confirmed to occur during mounting evaluation, the failure may not have been reproduced because the failure circumstances could not be simulated, or the failure may have been caused by some problem with device operation.

3.3.5 Non-destructive Internal Analysis of Packages

Methods of analyzing the internal structure of a device without opening the package include radiography, ultrasonic examination, and hermeticity evaluation.

3.3.5.1 Radiography

Radiography allows observation of the wire bonding condition (wire loop condition, arch shape and arch height). In addition, the wetting performance of the silver paste between the chip and die pad, and the presence of voids in the molded resin can be inspected.

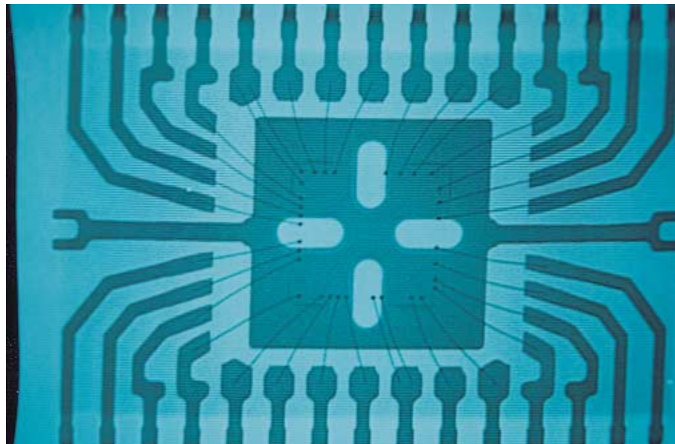


Photo 3-1 Radiography

3.3.5.2 Ultrasonic Analysis

Scanning acoustic tomographs (SAT) use ultrasonic waves (reflected waves) to enable non-destructive observation of the junction conditions at internal boundaries as shown in Fig. 3-2, and are used to evaluate solder heat resistance and other characteristics.

The SAT image is determined by the inherent acoustic impedance of each material at the junction boundary and the reflectivity R which depends on the material combination. When ultrasonic waves enter an area where the resin has been delaminated (air layer), the reflectivity is 100%, which provides a brighter picture than adhered portions. In addition, the reflected waveform phase is inverted at this time.

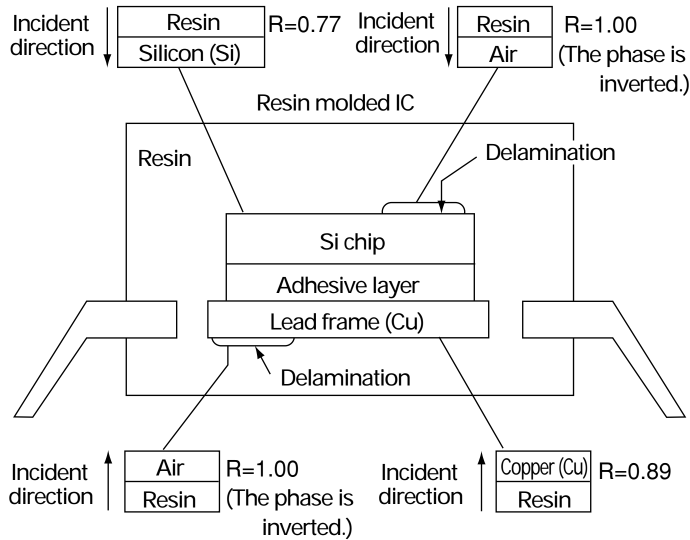


Fig. 3-2 Package Internal Junction Conditions and Reflection

Photo 3-2 shows an example of SAT analysis of a 28-pin SOP package.

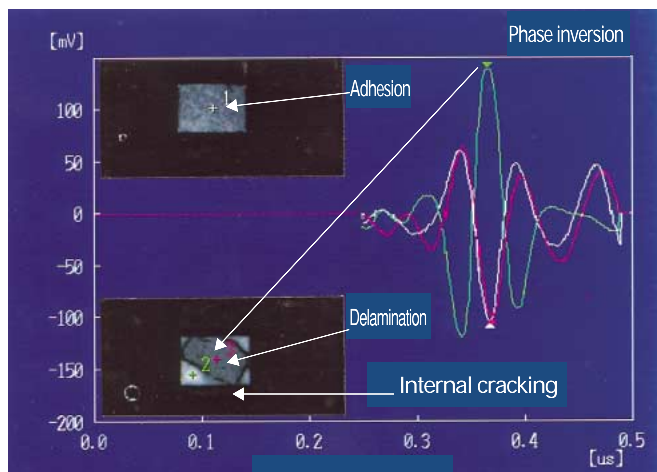


Photo 3-2 28-pin SOP Ultrasonic Analysis Diagram

Photo 3-3 shows a cross sectional SEM photo of a 28-pin SOP package.

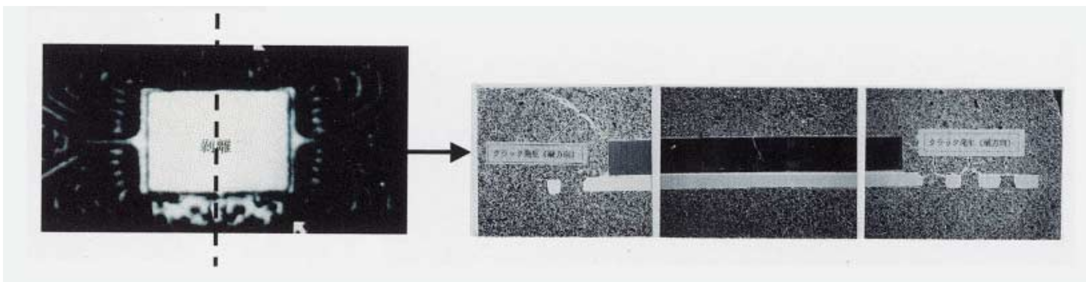


Photo 3-3 28-pin SOP Cross Sectional SEM Photo

The presence of delamination must be determined comprehensively by comparison with a reference sample in addition to the analysis image and reflected waveform (phase inversion).

As shown in Photo 3-2, internal cracking can also be checked by SAT analysis, but ultimately cutting and polishing of the cross section are necessary for the visual check.

3.3.5.3 Hermeticity Evaluation

Metal and ceramic type packages are hollow inside and sealed with nitrogen gas, and leakage must be limited to suppress the entry of moisture and impurities and corrosion of the aluminum pad. A leakage measurement method using helium is used to measure fine leaks.

3.3.6 Determining Failure Locations inside Chips

3.3.6.1 Description

When analyzing chip failures, the location of the failure inside the chip is first determined using failure locating technologies. Next, the form of the determined failure location is observed, and then composition analysis and other physical analysis are carried out to establish the cause of the failure.

Failure location uses the following methods.

The infrared radiation detection method is used to discover abnormal temperature distributions inside chips, the hot spot observation method is used to detect leaks using liquid crystals, and the photoemission method which detects feeble light emission is used to detect micro leaks, etc. Analysis of operating conditions includes the EBIC method which uses an electron microscope as a method of analyzing PN junction potentials, the OBIC method which uses a scanning laser microscope, and the voltage contrast method which analyzes wiring potentials using an EB tester.

These methods irradiate the chip surface with electron beams and detect light and other emissions from the chip surface, so the chip surface must be exposed while still in the package. Therefore, preparation such as decapping the package and removing the chip coating film is necessary.

3.3.6.2 Package Decapping Methods

Packages are decapped automatically using an acid decapsulator or manually by workers using tools. When using an acid decapsulator, decapping skill and experience are not required, and packages can be decapped easily even by unskilled workers. Photo 3-4 shows a 64-pin QFP package (chip size 3.6 × 3.6 mm) decapped using an acid decapsulator.

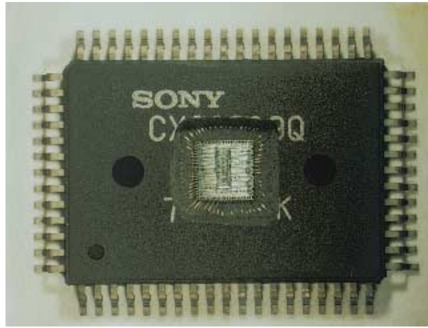


Photo 3-4 Package Decapping Example

There are a number of manual decapping methods using tools, and two examples are shown in Fig. 3-3 below. (a) shows the mold resin shaving method. Here, the resin over the chip is shaved with a grinder or drill, and the package is then immersed in a chemical solution to melt the resin. Dissolution is stopped when the chip becomes visible, and the package is then placed in an organic solvent and washed ultrasonically. This method immerses the entire package into the chemical solution, so the entire package surface melts. This method is used to decap DIP and other thick packages. (b) shows the acid resistant tape method.

Here, the package is covered with acid resistant tape, and the tape over the part to be melted is cut away. The package is then immersed in a chemical solution to melt the resin. Quartz is used to prevent lead bending. The acid resistant tape method melts only the target area, so packages can be decapped in an operable condition.

The acid resistant tape method is limited to QFP, SOP, BGA, CSP and other thin packages.

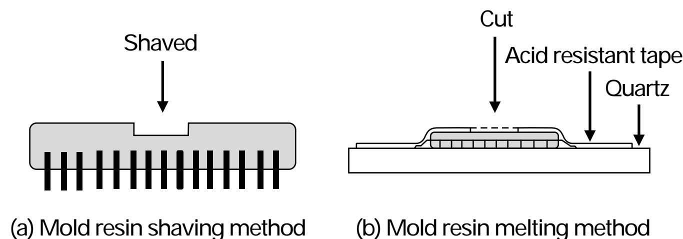


Fig. 3-3 Decapping Methods Using Tools

3.3.6.3 Fault Isolation

(1) Mechanical probing

This method contacts a fine metallic probe to the wiring inside the chip and measures the potential waveform of the internal wiring. This method has been used for quite some time, and it is the only method which can measure the absolute potential inside the chip.

In order to contact the metallic probe to the wiring, the wiring must be exposed to the chip surface. Therefore, the passivation film must generally be removed by plasma treatment.

To measure the signals in lower layer wiring, a hole is opened in the interlayer film using a focused ion beam (FIB), then a measurement pad is fabricated by depositing tungsten film and the probe is contacted to the wiring.

(2) Electron beam testing

This method irradiates a tightly focused electron beam to the chip surface and measures the potential distribution and voltage waveform in the internal wiring in the non-contact condition.

This method is non-contact, so high impedance measurement is possible and characteristics such as the waveform timing can be measured with high accuracy.

When an electron beam is irradiated to the chip surface, high energy secondary electrons are generated from the negative potential wiring and low energy secondary electrons are generated from the positive potential wiring. More secondary electrons are detected from the negative potential wiring than from the positive potential wiring, so the resulting contrast can be used to know the potential distribution over the wiring. (Photo 3-5) In addition, a voltage waveform can be obtained by fixing a pulse-converted electron beam at a single point on the wiring and detecting the potential information while shifting the timing at which the pulse beam is irradiated.

The information obtained from electron beam testing is waveforms and other logical information, so comparison with expected value information is necessary to determine the failure location. Therefore, methods such as comparing the potential distribution of good and defective chips or comparing actually measured waveforms with logical simulation waveforms are used to narrow down the failure location.

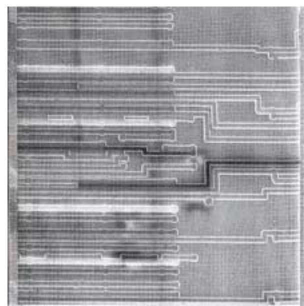


Photo 3-5 Potential Difference Analysis

(3) Photoemission analysis

This technique detects the feeble photoemissions produced by various types of failure on the chip surface using an emission microscope. Fig. 3-4 shows the photoemission analysis equipment configuration.

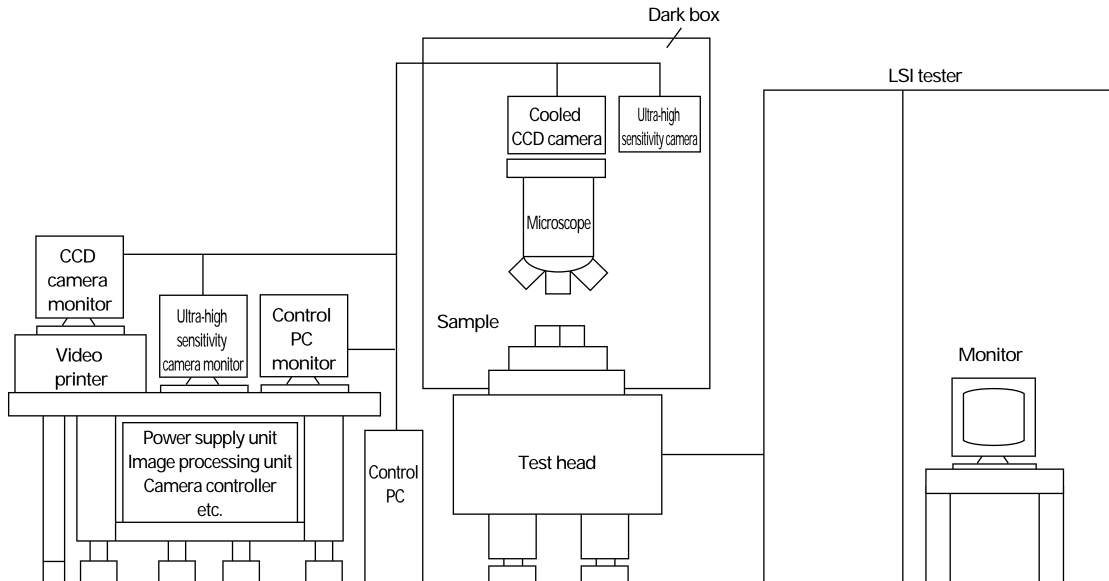
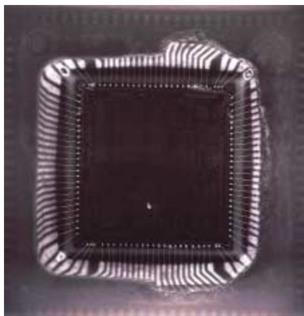


Fig. 3-4 Photoemission Analysis Equipment Configuration

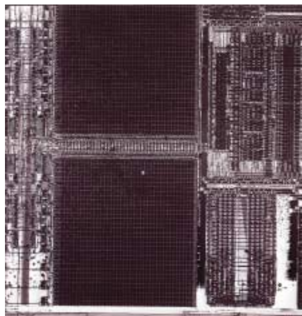
The photoemission image and the reflected image (optical microscope image) are captured by the same high sensitivity camera, and the photoemission positions on the chip can be detected by combining these two images into a single composite image. (Photo 3-6(a))

When a leak current flows to the gate oxide film or a PN junction, a high electric field region is created and photoemission caused by the micro plasma phenomenon is observed.

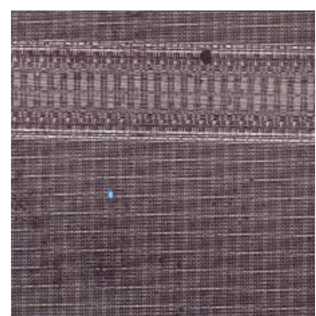
Furthermore, failure locations can also be narrowed down indirectly by observing hot electron emission from MOS transistors caused by open wiring connections and short circuits. Photoemission analysis is mainly used for leak failures, but the causes of function failures resulting from micro leaks can also be determined by detecting photoemissions from chips operated on an LSI tester. (Photo 3-6(b), (c)) In addition, the detection of photoemissions from the chip surface has become difficult for microcomputers, ASIC and other chips with multilayer metallic wiring, so these chips are analyzed by detecting infrared transmitted from the rear surface of the chip through the silicon.



(a) Entire chip



(b) Enlargement (block level)



(c) Enlargement (cell level)

Photo 3-6 Detection of Micro Leaks Using Photoemission Analysis

(4) Thermal emission analysis

Leak and short defect locations which emit heat can be detected using a liquid crystal. When heat is applied to a liquid crystal, transition of the liquid crystal occurs, and this can be observed using a polarizing microscope.

There are two analysis methods. The first method pre-heats the LSI to a temperature where the crystal properties of liquid crystals change. The second method uses the process of forcibly causing a transition in the liquid crystal and then bringing the liquid crystal back below the transition point by a combination of natural and forced cooling.

(5) OBIC (optical beam induced current) analysis

When semiconductors are irradiated by an optical beam, the phenomenon of light absorption by the semiconductor produces an excitation current. This excitation current changes at failure locations, so failure locations can be determined by detecting these changes. This method is called OBIC.

This method irradiates a laser beam having a specific wavelength as the light, and views changes in the device current as a visible image or a so-called current map image. (Photo 3-7)

Examples of application to failure analysis are as follows.

1. Detection of leak current locations
   (PN junction leaks, gate oxide film leaks, etc.)

2. Detection of abnormal standby current locations
3. Detection of ESD breakdown locations
4. Evaluation of latch-up
5. Observation of the depletion layer

Note that the optical excitation current differs according to the failure conditions and mode, but this current is extremely small, so periodically flowing current should be canceled and only the OBIC current should be analyzed with high sensitivity.

Current equipment can support levels as low as several 10 pA.

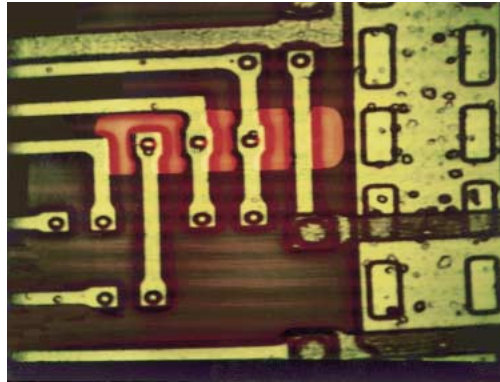


Photo 3-7 OBIC Analysis

3.3.7 Physical Analysis of Chips

Physical analysis of chips consists of observing the failure locations determined by the methods described thus far, and physically clarifying the cause of the failures.

Locations where the circuits comprising semiconductors have been damaged may be easily visible from the surface, but observation may be difficult when failures are located under other patterns. In these cases, the undesired patterns must be removed to facilitate observation.

Specific methods include removing patterns (exfoliation) from the upper surface layers to expose breakdown locations and causes, and exposing the cross section which contains the failure location. The appropriate method should be selected according to the results of electrical analysis, the exactness to which the location can be determined, and the results of surface observation from above the passivation film.

3.3.7.1 Exfoliation

This method removes the films in order from the passivation film, interlayer films, metal wiring and so on using methods appropriate to the film type. Care must be taken to apply as little damage as possible to the structure below the film to be removed, and to check and record the breakdown location exposure conditions at each stage.

Table 3-1 shows removal methods for various film types.

Table 3-1 Removal Methods for Various Film Types

Film type	Method	Chemicals and gases used
SiN	Dry etching	SF_6, N_2, O_2
	Wet etching	H_3PO_4
SiO_2	Dry etching	SF_6, N_2, O_2
	Wet etching	HF, CH_3COOH, SO-1 (HF, NH_4OH)
Al	Wet etching	HCl, H_2SO_4, H_2O_2
Ti/TiN/TiON	Wet etching	H_2SO_4, NH_4OH, H_2O_2
Poly Si	Wet etching	HF, HNO_3, CH_3COOH
	Ultrasonic washing	H_2O

3.3.7.2 Surface Observation (Optical Microscope, SEM)

In most cases, physical analysis starts from observation of the surface as this allows quick observation of a wide range. This method is used when exfoliating layers from the surface to expose failure locations.

Observation uses optical microscopes and scanning electrical microscopes (SEM).

In principle, optical microscopes use low magnification (up to approximately 2000×), but oxide films transmit light, so failure locations can sometimes be observed without exfoliation. In addition, interference colors are present depending on the thickness and refractive index of the transmitting film, so abnormalities during film forming can sometimes be detected by comparing the color with normal products.

SEM enable observation at magnifications of several ten to hundred thousand, and are indispensable for the physical analysis of semiconductors. Observed items include not only the external shape, but also conductivity and differences in formation from surrounding circuit elements. In addition, metal wiring which is floating electrically with respect to the silicon substrate is charged up and shines white, so contact defects and open connections can also sometimes be discovered.

3.3.7.3 Cross Sectional Observation (FIB, SEM)

Cross sectional observation is effective for determining the process in which foreign matter adhered and observing contact hole abnormalities. Methods used to expose the cross section include cutting, polishing, and focused ion beam (FIB). Observation normally uses SEM.

(1) Cleavage

This method splits the chip in the direction of the silicon crystals and observes the cross section. Depending on the observation target, slight etching may be performed using HF, H_2SO_4 or other etching agents to make contours easier to see. The observed location cannot be strictly determined, but this method is effective for observing repeated patterns and wide ranges.

(2) Polishing

Machining samples requires some time, but the cross sections at specific locations on chips can be observed more clearly than with FIB. First the chip is cut, then the piece containing the point to be observed is polished so that the cross section approaches the observation point. Polishing uses rough abrasives at first, and then switches to finer abrasive as the observation point is neared to prevent polishing mars, etc.

(3) FIB

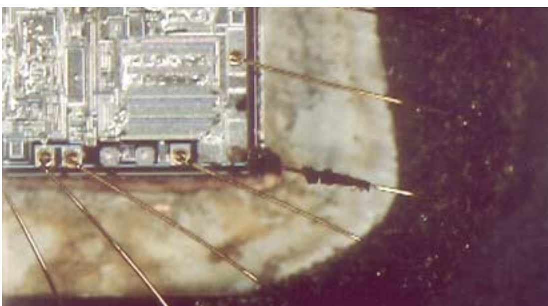
The chip surface is irradiated with a converged ion beam to etch the desired observation point on the chip and expose the cross section. The irradiated position can be determined while observing the image, so the cross section can be exposed with an accuracy of 1 μm or less.

3.3.7.4 Observation Points

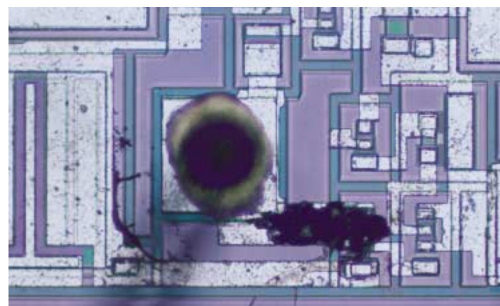
(1) Open connections, short circuits and leaks caused by excessive voltage and current

External surge voltages and currents may lead to open connections and short circuits. These failures mostly occur in the external input and output cells, but when surge voltages and currents cause latch-up, the aluminum wiring and gold wires used by internal cells may melt. (Photo 3-8)

Melting in the input and output cells can be easily confirmed by checking the electrical characteristics and observing from above the chip using a metallurgical microscope. However, internal cell melting requires careful observation with a metallurgical microscope, and polysilicon melting often occurs in the lower layers, so the upper layers must be exfoliated for observation.



(a) Open aluminum wiring connection inside a cell



(b) Open connection between the pad and aluminum wiring

Photo 3-8 Open Defects Caused by Excessive Voltage and Current

(2) Aluminum wiring corrosion

Moisture penetrating from outside the package, the formation of phosphoric acid, residual chlorine ions or other factors may cause aluminum corrosion resulting in open connections or short circuits between adjacent aluminum wiring. (Photo 2-11) Corroded aluminum wiring is often discolored, a condition which can easily be observed from above the passivation film using an optical microscope.

(3) Chip cracking (Photo 3-9)

Thermal stress may cause cracks in silicon chips, and these cracks have been confirmed to lead to electrical leaks between the power supply and GND in many cases.

Cracks may occur irregularly across the chip surface, or they may also occur along the grinding marks if grinding was insufficient or performed roughly during the rear surface grinding process. This failure mode can be easily discovered by observing the overall periphery of the chip using a metallurgical microscope. In addition, verification is also possible by removing the chip from the die pad and comparing the cracks with the grinding marks on the rear surface.

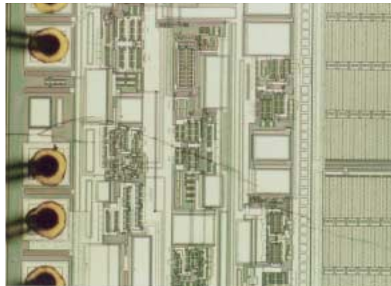


Photo 3-9 Chip Cracking

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(4) Mask alignment offset

This is when the diffusion area, polysilicon, contact holes, aluminum wiring, and via holes are offset relative to the upper or lower adjacent layers, and can be detected by surface observation. However, information such as the machining dimensions of each circuit element, the positional relation as viewed from the cross section, and the shape observation results are necessary to determine the cause of the failure.

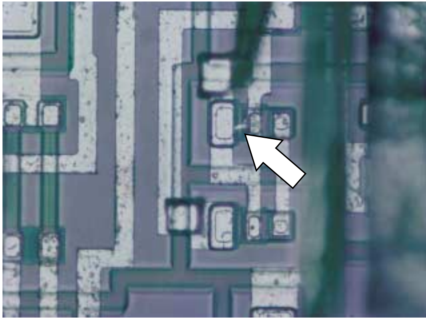
(5) Adherence of foreign matter

Foreign matter adhering within processes may cause slight deformations in the wiring or micro leaks. Continued use in this condition may lead to open connections or shorts due to electromigration. When the location of foreign matter is unclear, the surface layers must be exfoliated to allow observation, but when the location can be ascertained, the process in which the foreign matter adhered can be easily determined by observing the cross section with FIB, etc. In addition, the results of analyzing the shape and components of foreign matter also provide useful information for determining the cause.

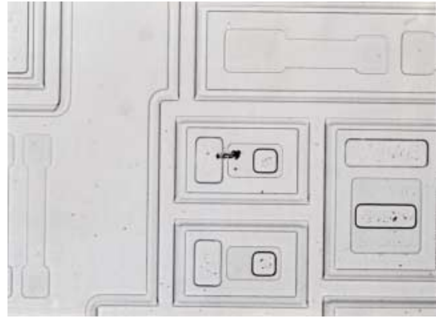
(6) Electrostatic breakdown (ESD)

The gate oxide film in current MOS devices is extremely thin, and these devices have low insulation strength. Therefore, when static electricity in excess of the IC endurance voltage is applied, breakdown results, and this phenomenon may manifest as short circuiting of the input and output pins. The breakdown mechanisms include aluminum wiring or polysilicon resistance burning, transistor gate oxide film damage, or junction damage, etc. Burning can be easily analyzed with a metallurgical microscope, but pinholes in the gate

oxide film require observation using SEM or other equipment. (Photo 3-10-(a), -(b))



(a) Aluminum wiring present



(b) Aluminum wiring removed

Photo 3-10 ESD Breakdown

(7) Electromigration and stress migration

Currents, temperature or mechanical stress within the manufacturing process or during use may cause a portion of the aluminum wiring surface to rise (hillock) or the wiring to crack (voids). Hillocks may cause short circuits with adjacent wiring to the side or above, or they may cause the passivation film to weaken and fail or the wiring to corrode.

Voids are caused by current-induced electromigration during use, and may result in increased resistance or open connections. Surface and cross sectional observation are used according to the analysis conditions.

3.3.8 Analysis and Structural Analysis Technologies

With increased LSI integration, cells are being miniaturized, and gate oxide films and capacitor insulating films are becoming thinner. Furthermore, multiple layers, trenches and other three-dimensional structures are making processes more complex and reducing manufacturing process margins. As a result, problems rooted in processes occur more easily, and make it difficult to ensure quality and reliability. Thus, analysis technologies are becoming more and more important in order to analyze process-related problems. The Sony Semiconductor Network Company has assembled the analysis technologies shown in Table 3-2 to assist in solving process-related problems.

Table 3-2 presents an overview of various analysis methods.

Table 3-2 List of Analysis Methods 1/3

	Analysis method	Measurement method	Obtained information	Measurement limits	Example measurement targets
Elemental Analysis	Ion Chromatography (IC)	Sample ion electrical conductivity	Ion presence and concentration in aqueous solutions	ppb level (ng/ml) to ppt level (pg/ml)	Inorganic anions and cations, organic ions
	Inductively Coupled Plasma Atomic Emission Spectroscopy (ICP-AES)	Light quantity emitted when atoms fall from an excited level to the normal level	Atomic concentration in solutions	ppb (ng/ml)〜 ppm (μg/ml)	Inorganic materials, acids, alkali, organic solvents
	Atomic Absorption Spectrometry (AA/FAA)	Light quantity absorbed by atoms	Metallic atom concentration in solutions	ppt(pg/ml) ppm (μg/ml)	Semiconductor materials, acids, alkali, organic solvents
	Inductively Coupled Plasma Mass Spectroscopy (ICP-MS)	Introduction of atomized plasma samples to a mass spectrometer	Atomic concentration in solutions and qualitative analysis of elements in solids	ppg (fg/ml)〜 ppt (pg/ml)	Inorganic materials, acids, alkalis, organic solvents, semiconductor materials
Chemical Structure Analysis	Fourier Transformation Infrared Spectroscopy (FT-IR)	Measurement of infrared absorption by substances at different wavelengths	Organic substance qualities and thin film quality	As small as several 10 μm in diameter	Organic materials, functional groups on semiconductor surfaces, etc.
	Visible Ultraviolet Spectroscopy (UV-VIS)	Measurement of ultraviolet or visible light transmittance through substances	Light transmittance of substances	0〜2Abs	Glass, organic materials, etc.
	Raman Spectroscopy	Measurement of inelastic scattering of light due to lattice and molecular vibration	Measurement of inelastic scattering of light due to lattice or molecular vibration	Area resolution as small as 8 μm	Semiconductor materials (Si, GaAs, etc.), organic and inorganic materials
	Gas Chromatography/ Infrared Spectroscopy/ Mass Spectroscopy (GC/IR/MS)	Measurement of substances separated by gas-liquid division using an infrared spectrophotometer and a mass spectrometer	Determination and quantitative analysis of the structure of gasified organic substances	ng level	Organic mixtures (solids, liquids, gases)
	Gas Chromatography/ Atomic Emission Detector (GC/AED)	Elemental analysis of substances separated by gas-liquid division using photoemission analysis	Elemental analysis of organic substances	ng level or less (depends on the element)	Organic mixtures

Table 3-2 List of Analysis Methods 2/3

	Analysis method	Measurement method	Obtained information	Measurement limits	Example measurement targets
Chemical Structure Analysis	Gas Chromatography/ Hydrogen Flame Ionization Detector (GC/FID)	Ionization of substances separated by gas-liquid division in a hydrogen flame and detection of the resulting current	Composition ratio of organic mixtures	10～100pg	Organic mixtures
	High Performance Liquid Chromatography (HPLC)	Measurement of substances by solid-liquid division using a pump	Separation of organic substances	Depends on the substance	Organic mixtures
	Fourier-Transform Nuclear Magnetic Resonance (NMR)	Electromagnetic wave absorption in a magnetic field by substances having a magnetic moment	Detailed structure, composition and relaxation time of substances having complex structures	Minimum weight ^{1}H nucleus: 0.1 mg, ^{13}C nucleus: 5 mg	Organic compounds, polymers, biological materials, catalysts
	High Resolution Mass Spectroscopy (HRMS)	Volatilized ionization	Molecular weight and molecular composition formula	Molecular weight: approximately 5,000	Organic materials
Thermal Analysis and Thermal Physical Properties	Thermal Analysis (TG, DSC, TMA) (TG-DTA)	Measurement of changes in mass, heat input and output, and expansion of substances while varying the temperature	Evaluation of thermal stability from the crystalline structure transmutation temperature and the thermal decomposition temperature of substances	Several mg of sample are required	Glass, polymer materials
	Thermal Desorption - Quadrupole Mass Spectroscopy (TD-QMS)	Detection of gas released from samples while increasing the temperature	Gas adsorption and crystal water desorption from substrates	Depends on the substance	Ceramics, metallic materials, etc.
Morphology Observation and Micro Analysis	Scanning Electron Microscopy (SEM)	Scanning a primary electron beam and observing the two-dimensional distribution of the secondary electron or reflected electron intensity	Sample surface shape, sample composition distribution image, and sample morphology image	Resolution: 0.7 to 0.3 nm	Solids, powders
	Electron Probe X-ray Micro Analysis (EPMA)	Measurement of the wavelength (energy) and intensity of characteristic X-rays generated by electron beam irradiation	Sample composition and in-plane distribution (mapping image)	0.1% ^{5}B to ^{92}U Resolution: 5 to 10 eV (WDX) or 150 eV (EDX)	Solids, powders
	Atomic Force Microscopy (AFM)	Measurement of the atomic force between the sample and probe	nm-order surface morphology (even for insulating objects)	0.01 nm (vertical), 2 to 3 nm (horizontal)	Semiconductor substrates, LSI interlayer films, organic thin films
	Surface Shape Measurement	Measurement of the surface shape with a contact probe	Solid surface steps and roughness	0.03 nm to 0.5 nm (vertical)	Evaporated thin film thickness, IC surface type oxide film etching patterns

Table 3-2 List of Analysis Methods 3/3

	Analysis method	Measurement method	Obtained information	Measurement limits	Example measurement targets
Surface Analysis	Auger Electron Spectroscopy (AES)	Measurement of the energy and intensity of Auger electrons generated by electron beam irradiation	Analysis of the composition and elements of several nm and thinner films in the depth direction	0.1%	Laser diode semiconductor samples, multilayer recording medium surface and interface analysis, composition changes
	X-ray Photoelectron Spectroscopy (XPS)	Measurement of the kinetic energy of photoelectrons emitted from the surface of solids by X-ray irradiation	Elemental composition and chemical bonding states to a depth several nm below the surface and analysis of these characteristics in the depth direction	0.1at%	Semiconductor, magnetic object and organic substance surfaces, various device surfaces
	Secondary Ion Mass Spectroscopy (SIMS)	Measurement of secondary ions released when solid samples are irradiated with ions	Mass spectrum, trace impurity density and distribution in the depth direction, and element distribution in the depth direction	10^{14}～10^{16} atoms/cm^3	Dopant profile in the depth direction inside semiconductor samples, elemental analysis of metal-semiconductor interfaces
Structural Analysis	Transmission Electron Microscopy (TEM)	Microscopy which enlarges images with an electromagnetic lens using the diffraction phenomenon of transmitted electrons	Crystalline structure, atomic arrangement, crystal defects, crystal orientation, magnetic domain structure, composition analysis and condition analysis	Point resolution: ≥ 0.19 nm Sample thickness: several nm to 300 nm or less	Semiconductor order structure, hetero-interfaces, ion implantation induced crystal defects, magnetic thin films, oxide superconductors
	Reflection High Energy Electron Diffraction (RHEED)	Irradiation of electrons along the surface and observing the diffraction map created by electrons diffracted by the surface	Crystal structure, orientation and damage at the top surface	Surface depth: several nm or less, measurement area beam diameter: 0.1 mm X sample size	Semiconductors, metallic thin films, magnetic materials (thin film bulk)
	X-ray Diffraction	Measurement of the diffraction angle and diffraction intensity of X-rays irradiated at samples	Lattice plane interval, crystalline structure, crystal properties, crystal orientation, residual stress (machining distortion)	10^{-3} at △d/d	Powders, polycrystalline films, epitaxial films, machined surfaces, adhering matter, magnetic films
	Pole figure Measurement	Tilting samples in various directions to investigate the X-ray diffraction intensity and crystal surface orientation	Distribution of crystal grain orientation in polycrystalline samples	Angular resolution > 2 °	Alloy films for magnetic heads, thin film magnetic mediums, coated tape, LSI wiring films
	X-ray Topography	Microscopy by irradiating X-rays and using the diffraction phenomenon to record imperfections inside crystals or at the crystal surfaces on a dry plate	Distribution of lattice defects (dislocations, precipitates, etc.) inside crystals, changes in lattice constants, lattice plane tilting	Resolution: several nm △d/d = 10^{-5} to 10^{-7}, 0.1 s	Semiconductor mono-crystals (Si, GaAs, etc.), magnetic crystals, optical crystals
	Laue Camera Method	Observation of white X-rays from mono-crystals and observation of the pattern symmetry	Crystal orientation	Angular resolution: 3 ° or less	Ferrite heads, optical crystals, semiconductors, metallic mono-crystals

3.3.8.1 Analysis of Metallic Impurities on Wafer Surfaces

Silicon wafer surface cleaning technology is essential for the manufacture of semiconductors, and contamination by metallic impurities is known to cause drops in the oxide film endurance voltage, increased leak current and other problems. Therefore, technology is needed to analyze impurity amounts of 10^8 to 10^9 atoms/cm^2 on wafer surfaces with high sensitivity.

In terms of chemical analysis methods, high sensitivity analysis was first made possible with the development of gaseous phase breakdown and atomic absorption photometry technologies, and improvements have since been made to the recovery method, which is where matters now stand. The recovery method distills hydrofluoric acid once and then takes metallic impurities into this highly pure hydrofluoric acid.

However, the purity of hydrofluoric acid has been improved to a level where there are presently no problems with its direct use. Therefore, the Sony Semiconductor Network Company has developed original contaminant metal dissolution and recovery technology called the indicator rod induction method. This method uses a small amount of highly pure hydrofluoric acid directly without distillation to allow the easy recovery of surface impurities. Fig. 3-5 shows an outline drawing of this technology.

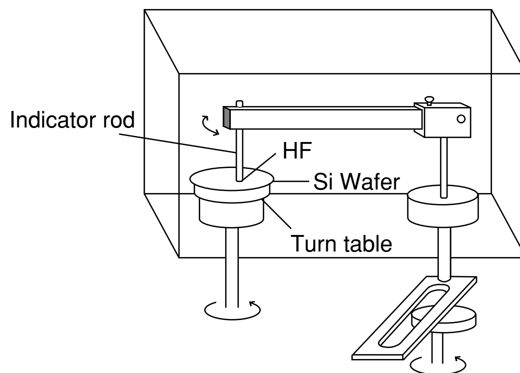


Fig. 3-5 Indicator Rod Induction Method Outline Drawing

The contaminant metal dissolution and recovery method first places a silicon wafer on a turntable, and then positions a 10 mm diameter indicator rod over the wafer with a gap of several millimeters. When 100 to 200 µl of highly pure hydrofluoric acid enters this gap, the surface tension keeps it within the gap and the wafer is rotated in this condition. On the other hand, the indicator rod has a mechanism which moves it back and forth over the wafer, and this moves the hydrofluoric acid evenly over the wafer in a spiral, making it possible to dissolve and absorb metallic impurities together with the natural surface oxide films into the hydrofluoric acid.

This simple recovery technology is combined with a high sensitivity atomic absorption photometer which uses a high luminance lamp to carry out analysis at the 10^8 atoms/cm^2 level and perform process line management.

An example of 9-element analysis performed after recovering the metallic contaminants from the surface of a washed 8-inch wafer using 200 µl of hydrochloric acid is shown below. Trace amounts of Na and K were detected, but all other elements were below the 10^8 atoms/cm^2 level detection limit.

Analysis of metallic impurities on the surface of a washed wafer ($\times 10^{10}$ atoms/cm^2)

Cr	Cu	Fe	K	Mg	Mn	Na	Ni	Zn
<0.04	<0.06	<0.03	0.16	<0.04	<0.01	0.38	<0.07	<0.05