
Description

The CXM3592UR is a high power and ultra-high linearity SPDT switch for wireless communication systems. This IC has a 1.8 V CMOS compatible decoder.

The Sony GaAs junction gate pHEMT(JPHEMT) MMIC process is used for low insertion loss and ultra-high linearity (Application: CDMA/LTE/GSM/UMTS Handsets and mini base stations)

Features

- ◆ Insertion Loss : 0.20 dB (typ.) (Cellular Band / GSM Low Band)
0.38 dB (typ.) (IMT2000 / GSM High Band)
- ◆ Ultra-High Linearity : IMD3 = -100 dBm (typ.) at LTE Band 13,
PTx = +23 dBm, PBlocker = +14 dBm
- ◆ Low voltage operation: $V_{DD} = 2.5$ V
- ◆ No DC blocking capacitors required on RF ports
- ◆ 1 control input
- ◆ Small package size: UQFN 12 pin (2.0 mm x 2.0 mm x 0.55 mm typ.)
- ◆ Lead-Free and RoHS compliant

Structure

GaAs JPHEMT MMIC switch, CMOS decoder

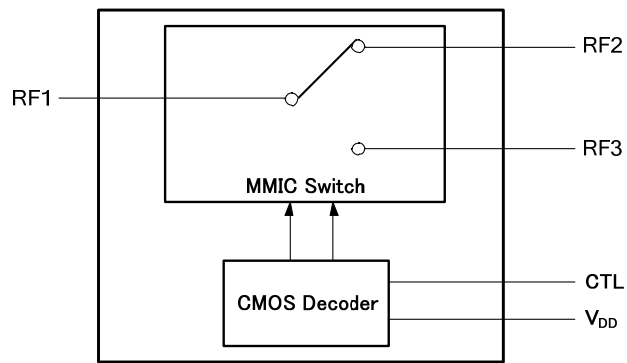
Absolute Maximum Ratings

Supply voltage	V_{DD}	4	V	$T_a = 25$ °C
Control voltage	V_{ctl}	4	V	$T_a = 25$ °C
Maximum input power		36	dBm	Duty cycle = 12.5 % to 50 %, $T_a = 25$ °C
Operating temperature	T_{opr}	-35 to +90	°C	
Storage temperature	T_{stg}	-65 to +150	°C	

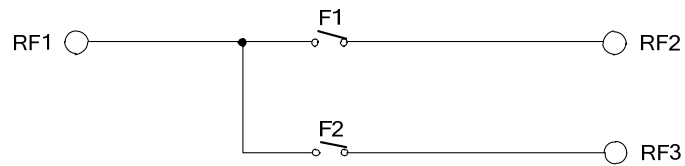
This IC is ESD sensitive device. Special handling precautions are required.

Block Diagram

SPDT Antenna Switch



RF Switch

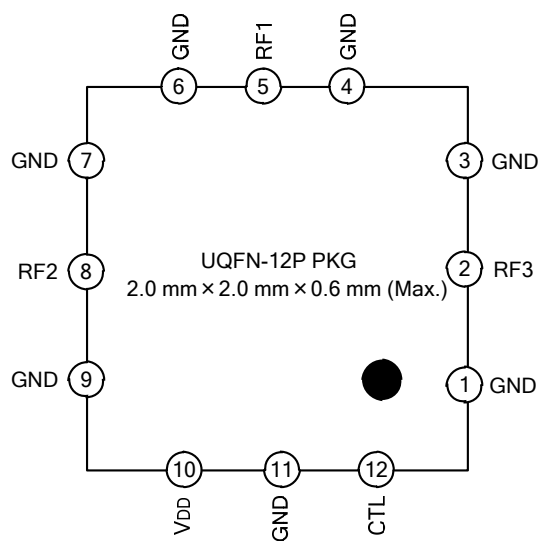


Truth Table

CTL	Active Path	F1	F2
L	RF1-RF2	ON	OFF
H	RF1-RF3	OFF	ON

Pin Configuration

(Top View)



DC Bias Condition

(Ta = 25 °C)

Parameter	Min.	Typ.	Max.	Unit
V _{DD}	2.5	2.7	3.3	V
V _{ctl} (H)	1.35	1.8	3.3	
V _{ctl} (L)	0	—	0.45	

Electrical Characteristics

(Ta = 25 °C, V_{DD} = 2.5 V, V_{ctl} = 0/1.8 V)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	RF1-RF2	*1, *2, *6, *8	—	0.20	0.35	dB
			*3, *4, *7, *9	—	0.38	0.53	
			*5	—	0.52	0.72	
		RF1-RF3	*1, *2, *6, *8	—	0.20	0.35	
			*3, *4, *7, *9	—	0.38	0.53	
			*5	—	0.52	0.72	
Isolation	ISO.	RF1-RF2	*1, *2, *6, *8	18	21	—	dB
			*3, *4, *7, *9	11	14	—	
			*5	9	12	—	
		RF1-RF3	*1, *2, *6, *8	18	21	—	
			*3, *4, *7, *9	11	14	—	
			*5	9	12	—	
VSWR	VSWR	All ports in active paths	700 to 2700 MHz	—	—	1.5	-
Harmonics	2fo	RF1-RF2, RF3	*6	—	-58	-41	dBm
	3fo			—	-62	-41	
	2fo		*7	—	-64	-45	
	3fo			—	-68	-45	
	2fo		*2, *3, *5	—	—	-50	
	3fo			—	—	-50	
	2fo			—	—	-78	
Inter modulation distortion in Rx Band	IMD2	RF1-RF2, RF3	*10, *11, *12, *15, *16, *19, *20, *23, *24	—	—	-110	dBm
	IMD3		*10, *13, *14, *17, *18, *21, *22, *25, *26	—	—	-110	dBm
			*10, *27, *29	—	-100	—	dBm
			*10, *28, *30	—	-100	—	dBm
Switching speed	T _s		50 % Ctl to 90 % RF	—	6.5	10	μs
Control current	I _{ctl}		V _{ctl} = 1.8 V	—	1	5	μA
Supply current	I _{dd}		V _{DD} = 2.7 V	—	0.14	0.35	mA

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

- * 1 Pin = 25 dBm, 704 to 787 MHz (Band 13, Band 17)
- * 2 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 8)
- * 3 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band 4 Tx)
- * 4 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)
- * 5 Pin = 26 dBm, 2500 to 2690 MHz (Band 7)
- * 6 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)
- * 7 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)
- * 8 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)
- * 9 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)
- * 10 Measured with the recommended circuit.

IMD condition (1)

Band	fRx on RF [MHz]	fTx +20 dBm on RF [MHz]	fBlocker -15 dBm on RF1 [MHz]		IMD condition
Band 1	2140	1950	IMD2(fRx - fTx)	190	*11
			IMD2(fRx + fTx)	4090	*12
			IMD3(2fTx - fRx)	1760	*13
			IMD3(2fTx + fRx)	6040	*14
Band 2	1960	1880	IMD2(fRx - fTx)	80	*15
			IMD2(fRx + fTx)	3840	*16
			IMD3(2fTx - fRx)	1800	*17
			IMD3(2fTx + fRx)	5720	*18
Band 5	880	835	IMD2(fRx - fTx)	45	*19
			IMD2(fRx + fTx)	1715	*20
			IMD3(2fTx - fRx)	790	*21
			IMD3(2fTx + fRx)	2550	*22
Band 7	2655	2535	IMD2(fRx - fTx)	120	*23
			IMD2(fRx + fTx)	5190	*24
			IMD3(2fTx - fRx)	2415	*25
			IMD3(2fTx + fRx)	7725	*26

IMD Condition (2)

Band	fRx on RF [MHz]	fTx PTx=+23 dBm on RF [MHz]	fBlocker PBlocker = +14 dBm on RF1 [MHz]		IMD condition
Band 13	747	786	IMD3(2fTx - fRx)	825	*27
BC0	872	827	IMD3(2fTx - fRx)	782	*28

IMD Condition (3)

Band	fRx on RF [MHz]	fTx PTx=+24 dBm on RF [MHz]	fBlocker PBlocker = +13 dBm on RF1 [MHz]		IMD condition
Band 13	747	786	IMD3(2fTx - fRx)	825	*29
BC0	872	827	IMD3(2fTx - fRx)	782	*30

Triple Beat Ratio

(Ta = 25 °C, V_{DD} = 2.5 V, V_{ctl} = 0/1.8 V)

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit	
Triple beat ratio	TBR		Input power at RF [dBm]	Tx1 at RF* [MHz]	Tx2 at RF* [MHz]	Jammer at RF1 -30 dBm [MHz]	Triple beat product at RF* [MHz]				dBc
		RF1 - RF2, RF3	21.5	835.5	836.5	881.5	881.5±1	81	—	—	
			21.5	1880	1881	1960	1960±1	81	—	—	
		13.5	1732	1733	2132	2132±1	81	—	—		

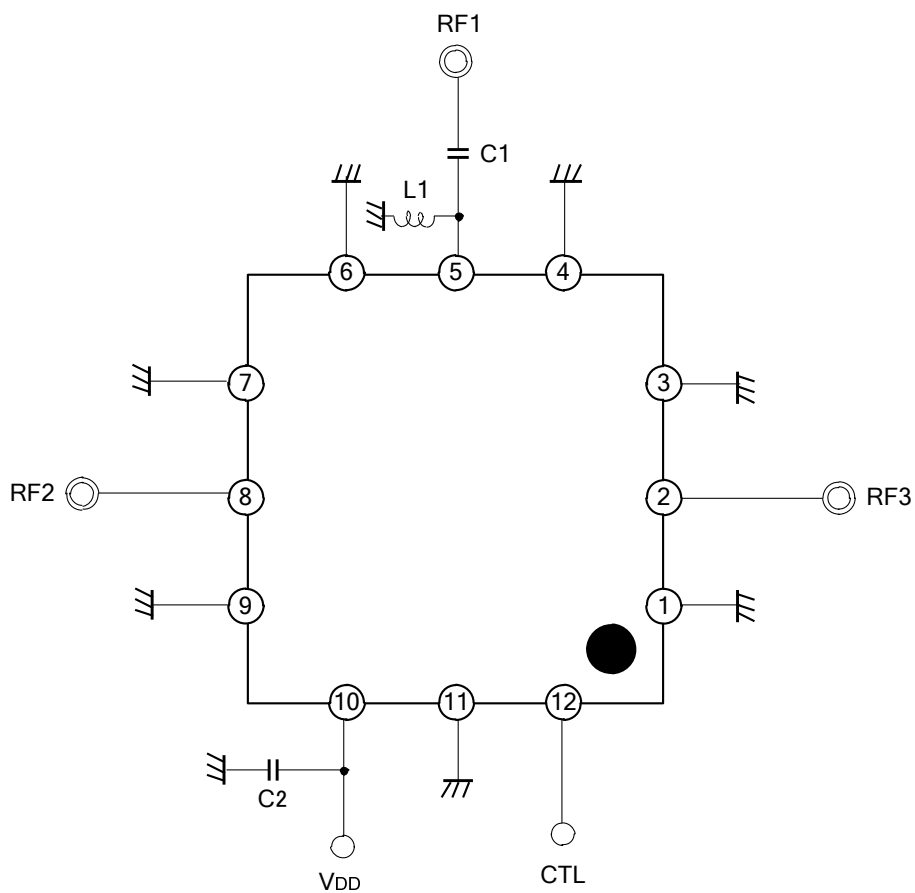
*Electrical characteristics are measured with all RF ports terminated in 50 Ω
 Measured with the recommended circuit.

IIP2

(Ta = 25 °C, V_{DD} = 2.5 V, V_{ctl} = 0/1.8 V)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
Input IP2	IIP2		Tx at RF* 26 dBm [MHz]	Jammer at RF1 -20 dBm [MHz]	IM2 Product at RF* [MHz]				dBm
		RF1 - RF2, RF3	836.61	1718.61	881.61	113.5	—	—	
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
1732.5	400		2132.5	95.5	—	—			

*Electrical characteristics are measured with all RF ports terminated in 50 Ω
 Measured with the recommended circuit.

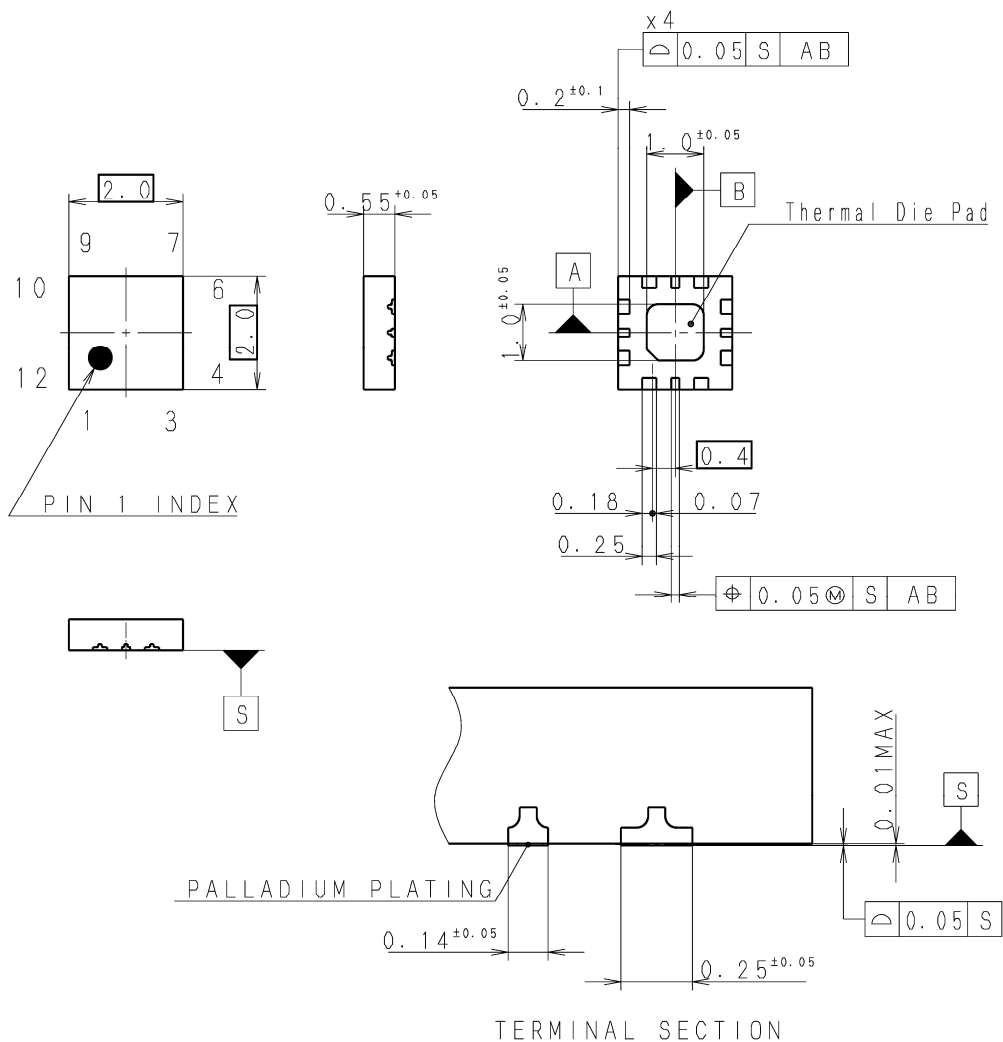
Recommended Circuit

- *1 No DC blocking capacitors are required on all RF ports.
- *2 The DC levels of all RF ports are GND.
- *3 L1 (27 nH) and C1 (12 pF) are recommended on RF 1 port for ESD protection.
- *4 C2 (100pF) is recommended on VDD pin for Decoupling Capacitor .

Package Outline

(Unit: mm)

12PIN UQFN (PLASTIC)



Note: Terminal burr height 0.05mm MAX.

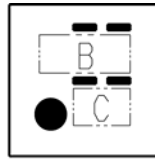
PACKAGE STRUCTURE

SONY CODE	UQFN-12P-03
JEITA CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.006g

PART No.	AP-4000-12011S	Rev. 0
ISSUED	/ 11.06.14	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR KYUSHU	
REMARKS	PKG CODE: UR-12-A	

Marking



MARKING C: GF

注1) B部はロット番号 (Max 3文字で通し記号) を配置する。

(規定文字数未滿につき省略は省略規定に従う。)

製造年は下記2進法ビット方式により表示する。)

a 部年コード (2進法ビット方式の1ビット目を表示) を配置する。

b 部年コード (2進法ビット方式の2ビット目を表示) を配置する。

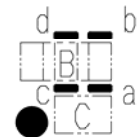
c 部年コード (2進法ビット方式の3ビット目を表示) を配置する。

d 部年コード (2進法ビット方式の4ビット目を表示) を配置する。

注2) C部は製品名 (Max 2文字) を配置する。

(2文字を超える場合は製品名省略標示規定に従う。)

注3) マーク深さは、Max 0.05mmの事。



DETAIL B

< INSTRUCTIONS >

1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.

(FOLLOW RULES FOR ABBREVIATIONS.

MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)

A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.

A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.

A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.

A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.

2) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.

(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

3) MARK DEPTH MAX 0.05 mm.

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.