
Description

The CXD5400 is a module for the GPS (Global Positioning System), satellite-based location measurement system. This module enables the configuration of high-sensitivity GPS/SBAS receiver system providing a cost reduction and low-power solution.

This module is available by providing power supply for the interface with main power supply and HOST LSI only, not requiring external elements and components because it incorporates GPS receiver LSI, TCXO, crystal oscillator for RTC etc.

Features

- ◆ Integrated power control by internal LDO, DC/DC Converter etc.
- ◆ Strong noise immunity by internal digital filter
- ◆ Development support function by internal FFT analyzer
- ◆ External clock input not required by incorporated crystal oscillator for TCXO and RTC
- ◆ HOST interface provided by UART · I²C
- ◆ I²C interface provided for connecting with acceleration and terrestrial magnetism sensor etc.
- ◆ Reduced cost related to BOM by incorporating all of capacitors and inductors for RF circuit and each LDO
- ◆ Incorporated LNA and SAW filter realize high-sensitivity and noise immunity
- ◆ Communication by NMEA-0183 from HOST interface
- ◆ 7.5 mm x 9.5 mm space-saving footprint

Package

35-pin LGA

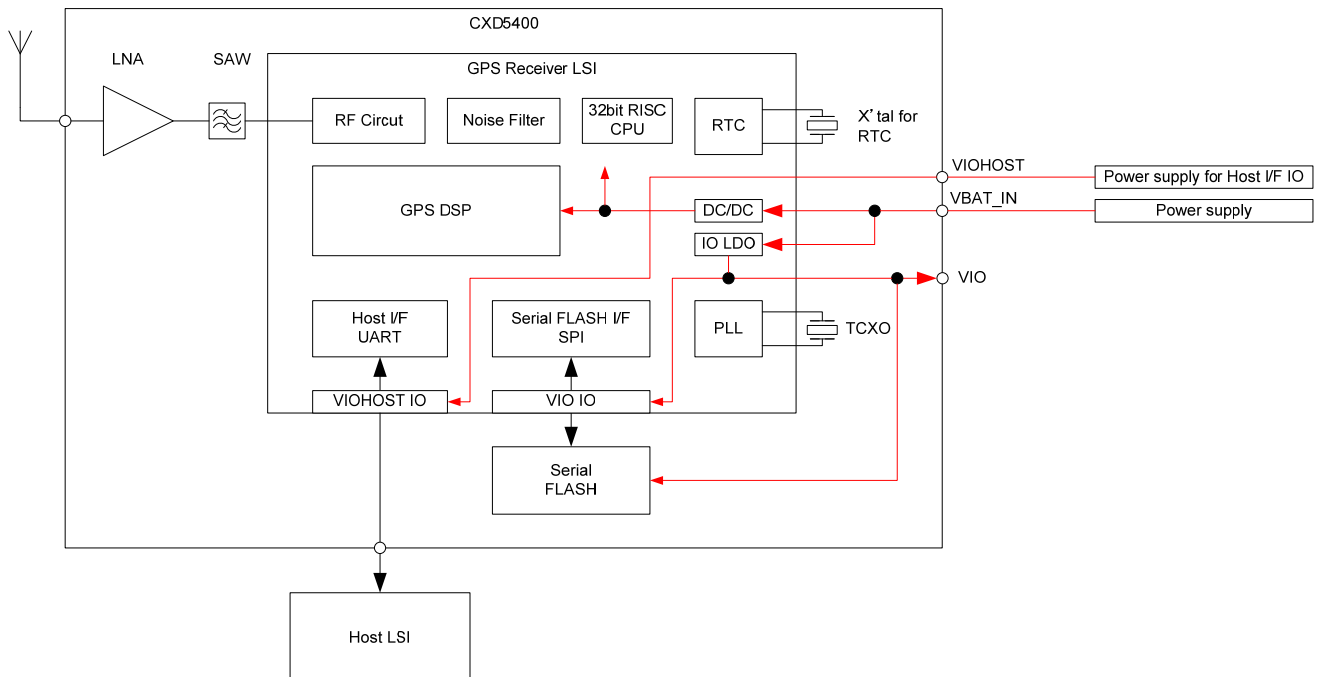
Absolute maximum ratings

Pin · Item	Min.	Max.	Unit
VBAT_IN	-0.3	4.5	V
VIOHOST	-0.3	3.6	V
PWR_EN, PWR_EN_BCKUP	0	4.5	V
RF Input Power	-	5	dBm
Pins other than above	-0.3	3.6	V
Storage temperature	-40	85	°C
Operating Conditions	-25	80	°C

Recommended Operating Conditions

Item	Min.	Max.	Unit
VBAT_IN voltage	2.7	4.3	V
VIOHOST voltage	1.62 to 3.63		V

Block Diagram



Description of Functions

Receiver performance

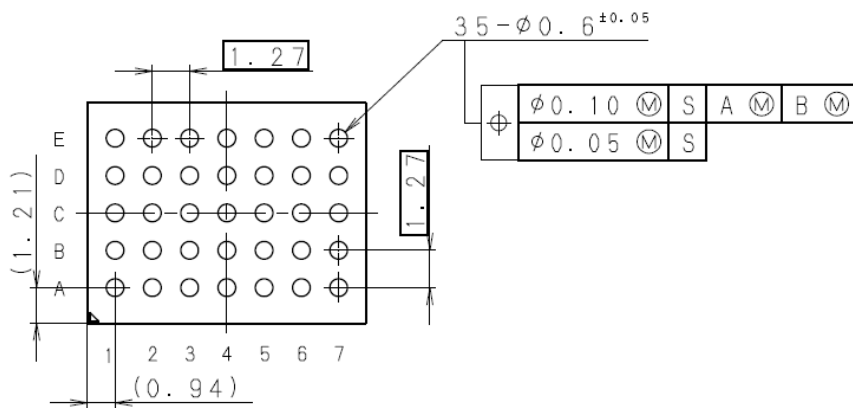
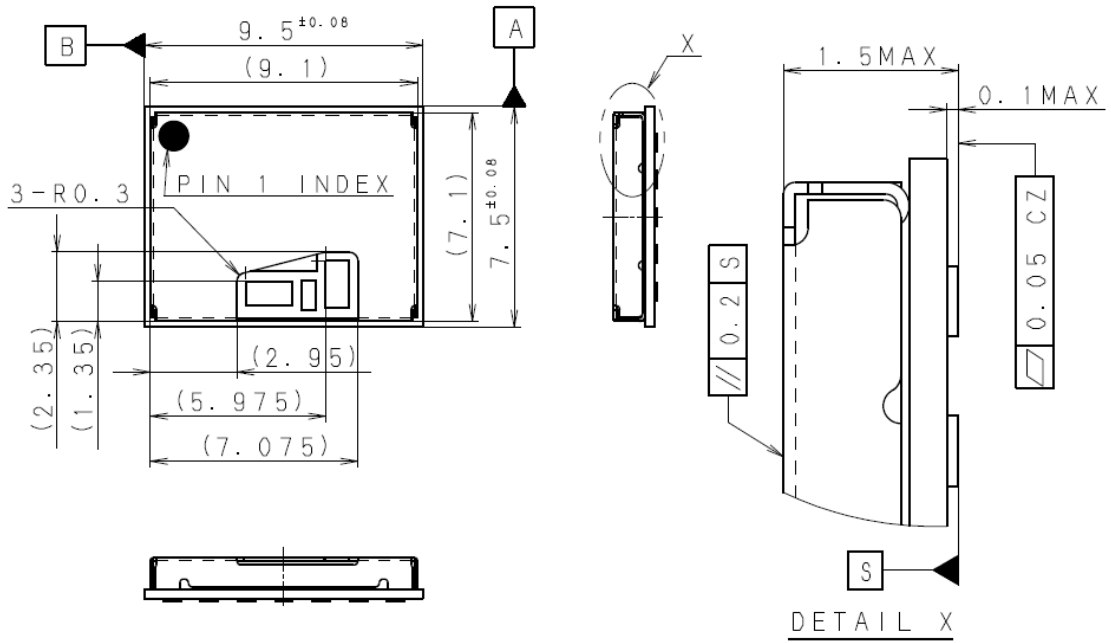
- Tracking sensitivity -165 dBm
- Hot start sensitivity -155 dBm
- Cold/warm start -148 dBm
- Warm start TTFF (-130 dBm) 33 s
- Hot start TTFF (-130 dBm) 1 s

Power consumption

- When tracking 74 mW (typ.)
- When acquisition 81 mW (typ.)
- When backup mode (PWR_EN = Low, PWR_EN_BCKUP = High) 1 mW or less
- When off mode (PWR_EN, PWR_EN_BCKUP = Low) 1 mW or less

Package Outline

35PIN LLGA



Note

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