SONY

CXG7001FN

Power Amplifier/Antenna Switch + Low Noise Down Conversion Mixer for PHS

Description

The CXG7001FN is a MMIC consisting of the power amplifier, antenna switch and low noise down conversion mixer.

This IC is designed using the Sony's GaAs J-FET process featuring a single positive power supply operation.

Features

- Operates at a single positive power supply: V_{DD} = 3V
- Small mold package: 26-pin HSOF

<Power amplifier/antenna switch transmitter block >

- Low current consumption: I_{DD} = 150mA (P_{OUT} = 20.2dBm, f = 1.9GHz)
- High power gain: Gp = 39dB Typ. (P_{OUT} = 20.2dBm, f = 1.9GHz)

<Antenna switch receiver block/ low noise down conversion mixer>

- Low current consumption: I_{DD} = 5.5mA Typ. (When no signal)
- High conversion gain: Gc = 20.5dB Typ. (f = 1.9GHz)
- Low distortion: Input IP3 = –13dBm Typ. (f = 1.9GHz)
- High image suppression ratio: IMR = 40dBc Typ. (f = 1.9GHz)
- High 1/2 IF suppression ratio: 1/2IFR = 44dBc Typ. (f = 1.9GHz)

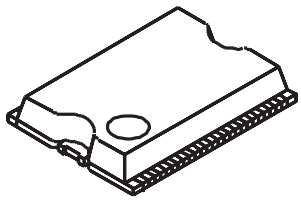
Applications

Japan digital cordless telephones (PHS)

Structure

GaAs J-FET MMIC

26 pin HSOF (Plastic)



Absolute Maximum Ratings

<Power amplifier block>			
• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	V_{GSO}	1.5	V
• Gain control voltage	VP_{CTL}	2.5	V
• Drain current	I_{DD}	550	mA
• Allowable power dissipation	P_D	3	W
<Switch block>			
Control voltage	V_{CTL}	6	V
<Front-end block>			
• Supply voltage	V_{DD}	6	V
• Input power	P_{RF}	+10	dBm
<Common to each block>			
• Channel temperature	Tch	150	°C
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

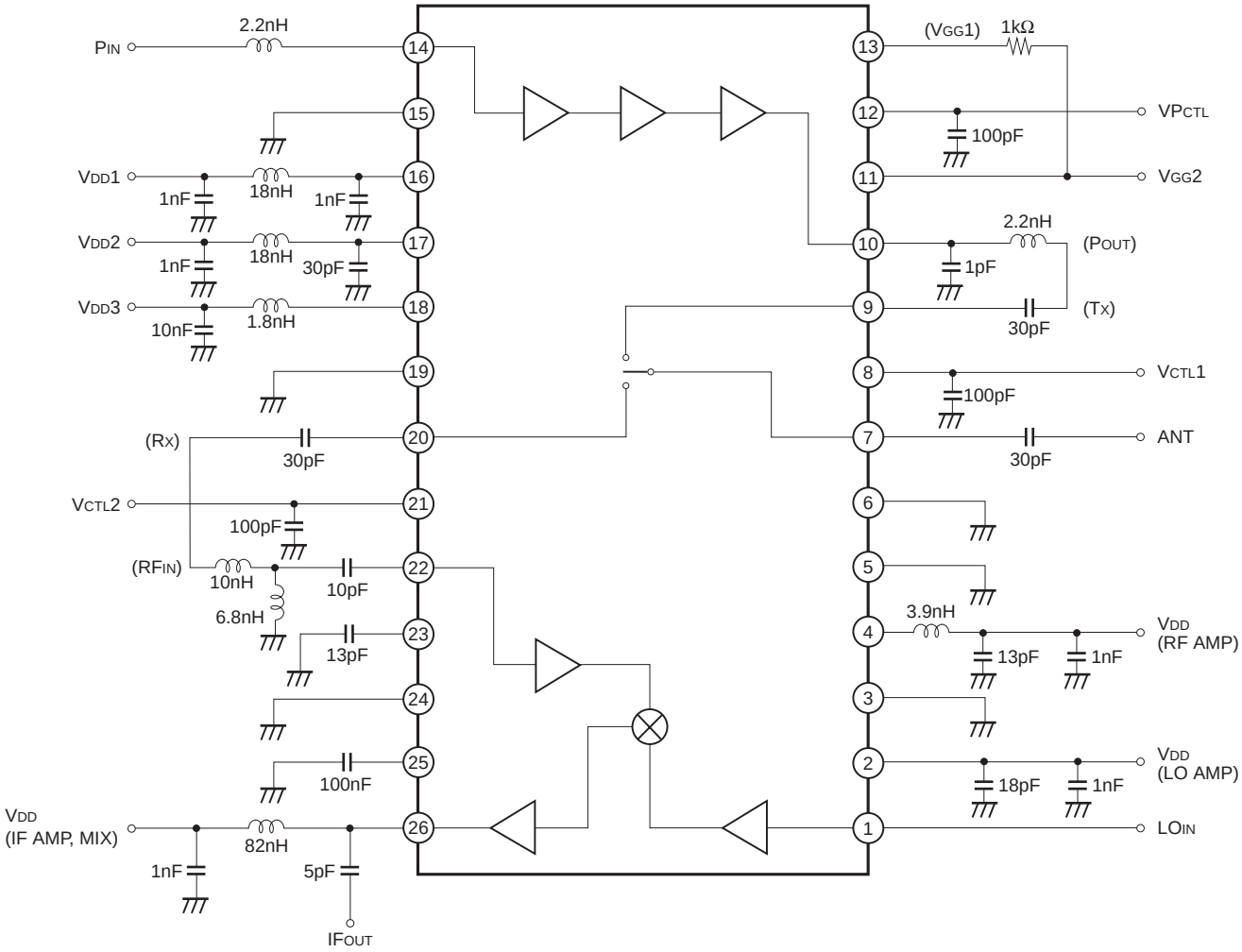
<Common to each block>			
• Supply voltage	V_{DD}	2.7 to 3.3	V
<Power amplifier block>			
• Gain control voltage	VP_{CTL}	to V_{DD}–1.0	V
<Switch block>			
• Control voltage (H)	V_{CTL} (H)	2.9 to 3.3	V
• Control voltage (L)	V_{CTL} (L)	0 to 0.2	V

Notes on Handling

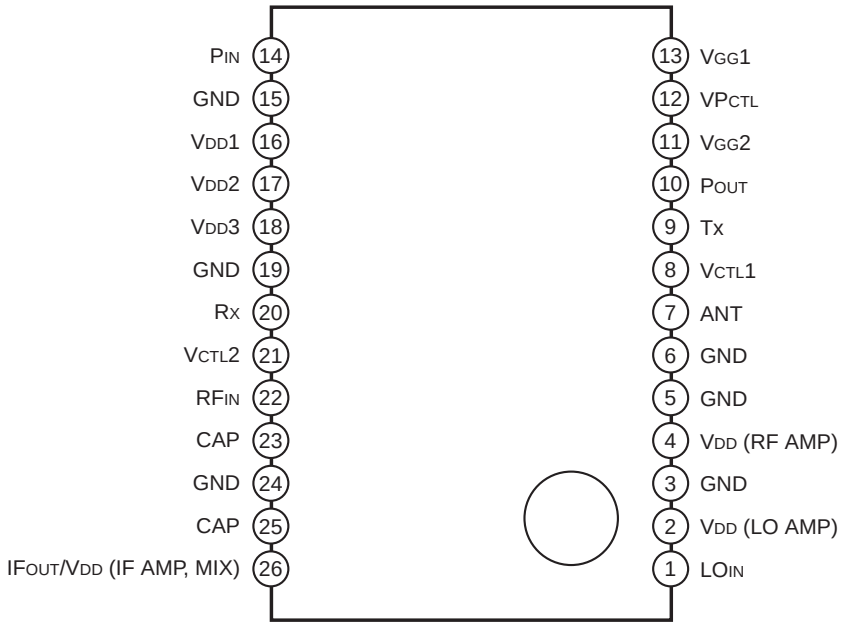
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E04139-PS

Block Diagram and External Circuit



Pin Configuration



26 pin – HSOF (Plastic)

Pin Description

Pin No.	Symbol	Description
1	LO_{IN}	LO signal input.
2	V_{DD} (LO AMP)	LO AMP V_{DD}.
3	GND	GND.
4	V_{DD} (RF AMP)	RF AMP V_{DD}.
5	GND	GND.
6	GND	GND.
7	ANT	Antenna switch. Either ANT-Tx or ANT-Rx is depending on whether the setting is VCTL1 or VCTL 2.
8	$V_{CTL}1$	Antenna switch control Pin 1.
9	T_X	Tx. Input the signal into the antenna switch when ANT-Tx.
10	P_{OUT}	Power amplifier output.
11	$V_{GG}2$	Power amplifier (the final-stage FET) gate voltage adjustment Pin 2.
12	VP_{CTL}	The first-stage FET control pin for the power amplifier.
13	$V_{GG}1$	Power amplifier (the first-stage FET, the second-stage FET) gate voltage adjustment Pin 1.
14	P_{IN}	Signal input into the power amplifier.
15	GND	GND.
16	$V_{DD}1$	Power amplifier (the first-stage FET) $V_{DD}1$.
17	$V_{DD}2$	Power amplifier (the second-stage FET) $V_{DD}2$.
18	$V_{DD}3$	Power amplifier (the final-stage FET) $V_{DD}3$.
19	GND	GND.
20	R_X	Rx. Output ANT input signal into Rx when ANT-Rx.
21	$V_{CTL}2$	Antenna switch control Pin 2.
22	RF_{IN}	RF signal input.
23	CAP	Connector for the external capacitor. Connected to LNA FET source. Self-vibration frequency becomes 1.9GHz by this capacitor (Typ. 13pF).
24	GND	GND.
25	CAP	Connector for the external capacitor. IF AMP distortion is corrected by this capacitor.
26	IF_{OUT}/V_{DD} (IF AMP, MIX)	IF output and IF AMP, MIX V_{DD}.

Electrical Characteristics

1. Control Pin Logic for Antenna Switch

Conditions of control pins	ANT – T_X	ANT – R_X
$V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V	ON	OFF
$V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V	OFF	ON

2. Power Amplifier Block + Antenna Switch Transmitter Block

These specifications are those when the Sony's recommended evaluation board, shown on page 7, is used.

Unless otherwise specified: V_{DD} = 3V, VP_{CTL} = 2V, $V_{CTL}1$ = 3V, $V_{CTL}2$ = 0V,
I_{DD} = 150mA, P_{OUT} = 20.2dBm, f = 1.9GHz, Ta = 25°C

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}			150		mA
Gate voltage adjustment value	V_{GG}		0.04	0.25	0.60	V
Output power	P_{OUT}	Measured with the ANT pin	20.2			dBm
Power gain	G_P		36	39		dB
Adjacent channel leak power ratio (600 ± 100kHz)	ACPR600kHz	Measured with the ANT pin		–63	–55	dBc
Adjacent channel leak power ratio (900 ± 100kHz)	ACPR900kHz	Measured with the ANT pin		–70	–60	dBc
Occupied bandwidth	OBW	Measured with the ANT pin		250	275	kHz
2nd-order harmonic level	—	Measured with the ANT pin			–25	dBc
3rd-order harmonic level	—	Measured with the ANT pin			–25	dBc

3. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer Block

These specifications are those when the Sony's recommended evaluation board, shown on page 7, is used.

Unless otherwise specified: V_{DD} = 3V, $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V, RF1 = 1.90GHz/–35dBm,
LO = 1.66GHz/–15dBm, Ta = 25°C

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}	When no signal		5.5	7.5	mA
Conversion gain	G_C	When a small signal	17	20.5		dB
Noise figure	NF	When a small signal		4.2	5.5	dB
Input IP3	IIP3	*1	–17.5	–13		dBm
Image suppression ratio	IMR	RF2 = 1.42GHz/–35dBm	30	40		dBc
1/2 IF suppression ratio	1/2IFR	RF2 = 1.78GHz/–35dBm	39	44		dBc
2 × LO–IF suppression ratio	—	RF2 = 3.08GHz/–35dBm	39	47		dBc
2 × LO+IF suppression ratio	—	RF2 = 3.56GHz/–35dBm	24	62		dBc
LO to ANT leak	P_{LK}			–42	–37	dBm

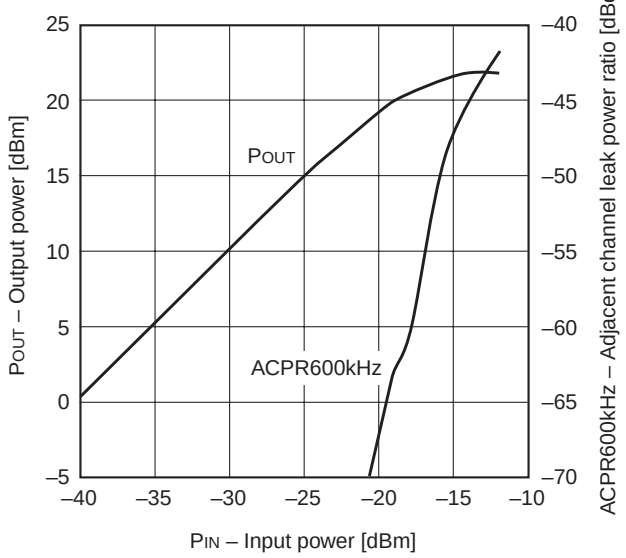
*1 Conversion from IM3 suppression ratio during FR1 = 1.9000GHz/–35dBm and FR2 = 1.9006GHz/–35dBm input.

Example of Representative Characteristics

1. Power Amplifier + Antenna Switch Transmitter Block (f = 1.9GHz, Ta = 25°C)

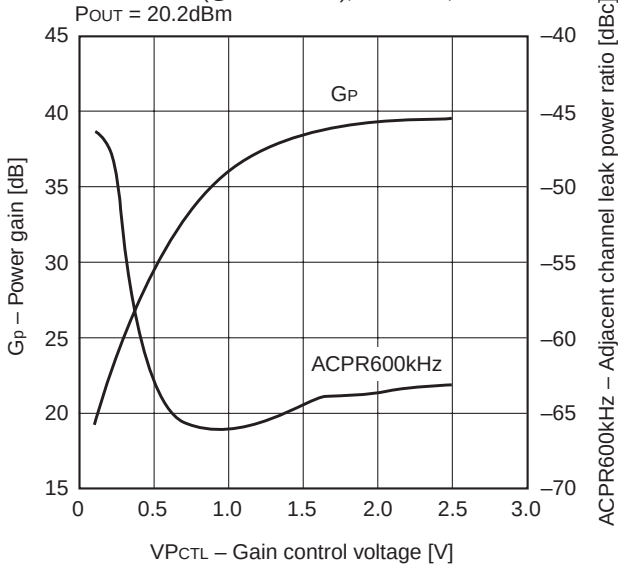
POUT, ACPR600kHz vs. PIN

VDD = 3V, VPCTL = 2V, VGG = const., VCTL1 = 3V,
VCTL2 = 0V
IDD = 150mA (@POUT = 20.2dBm), PIN = var.



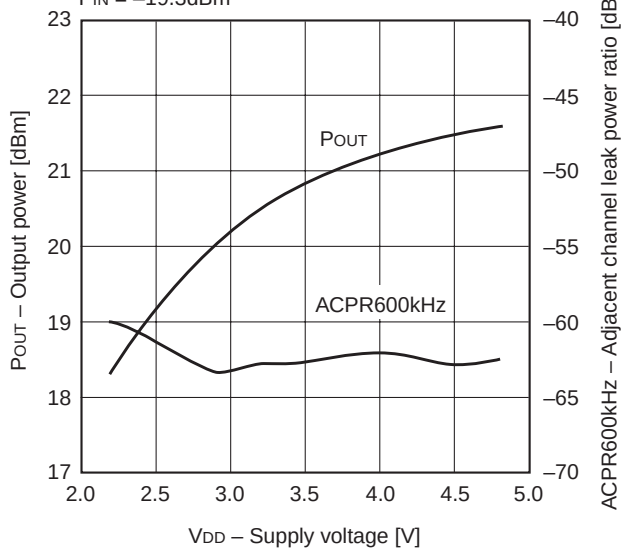
Gp, ACPR600kHz vs. VPCTL

VDD = 3V, VPCTL = var., VGG = const., VCTL1 = 3V,
VCTL2 = 0V
IDD = 150mA (@VPCTL = 2V), PIN = var.,
POUT = 20.2dBm



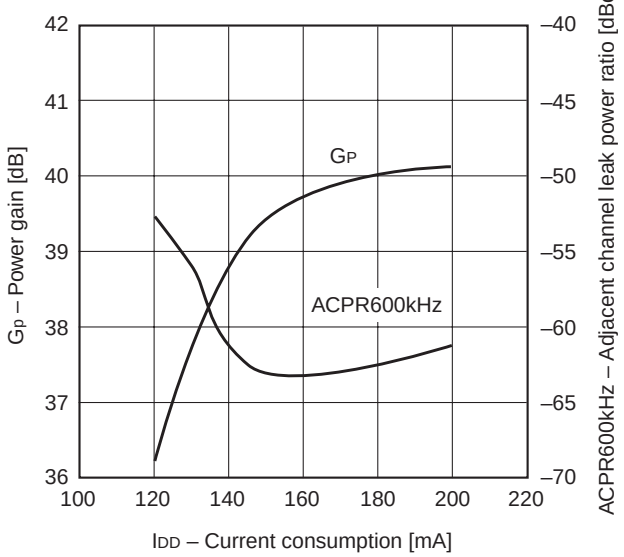
POUT, ACPR600kHz vs. VDD

VDD = var., VPCTL = 2V, VGG = const., VCTL1 = 3V,
VCTL2 = 0V
IDD = 150mA (@VDD = 3V, POUT = 20.2dBm),
PIN = –19.3dBm



Gp, ACPR600kHz vs. IDD

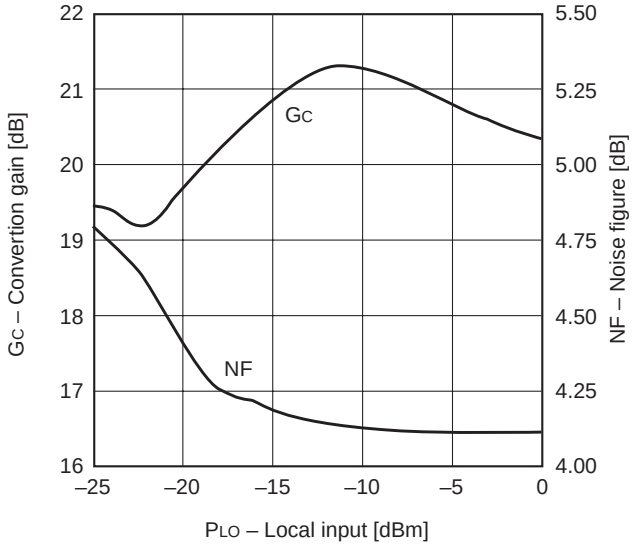
VDD = 3V, VPCTL = 2V, VGG = var., VCTL1 = 3V,
VCTL2 = 0V
IDD = var., PIN = var., POUT = 20.2dBm



2. Antenna Switch Receiver Block + Low Noise Down Conversion Mixer (Ta = 25°C)

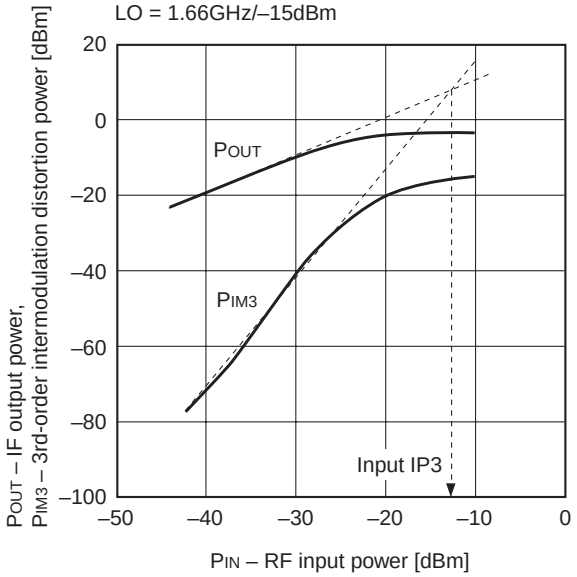
GC, NF vs. PLO

VDD = 3V, VCTL1 = 0V, VCTL2 = 3V,
RF = 1.90GHz/small signal, LO = 1.66GHz



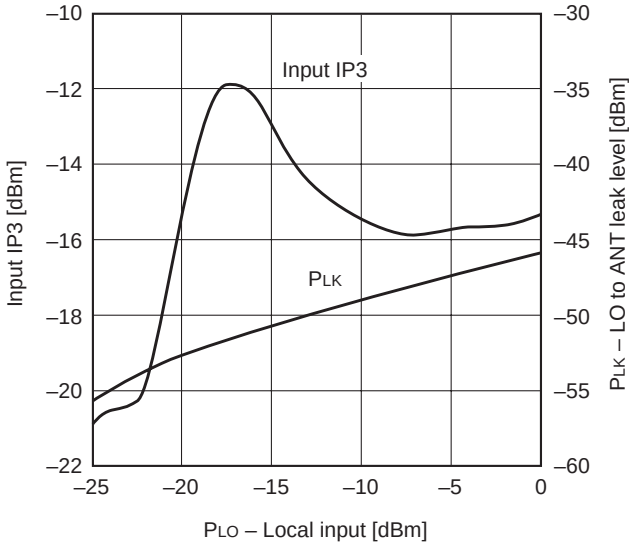
POUT, PIM3 vs. PIN

VDD = 3V, VCTL1 = 0V, VCTL2 = 3V,
RF1 = 1.9000GHz, RF2 = 1.9006GHz,
LO = 1.66GHz/–15dBm

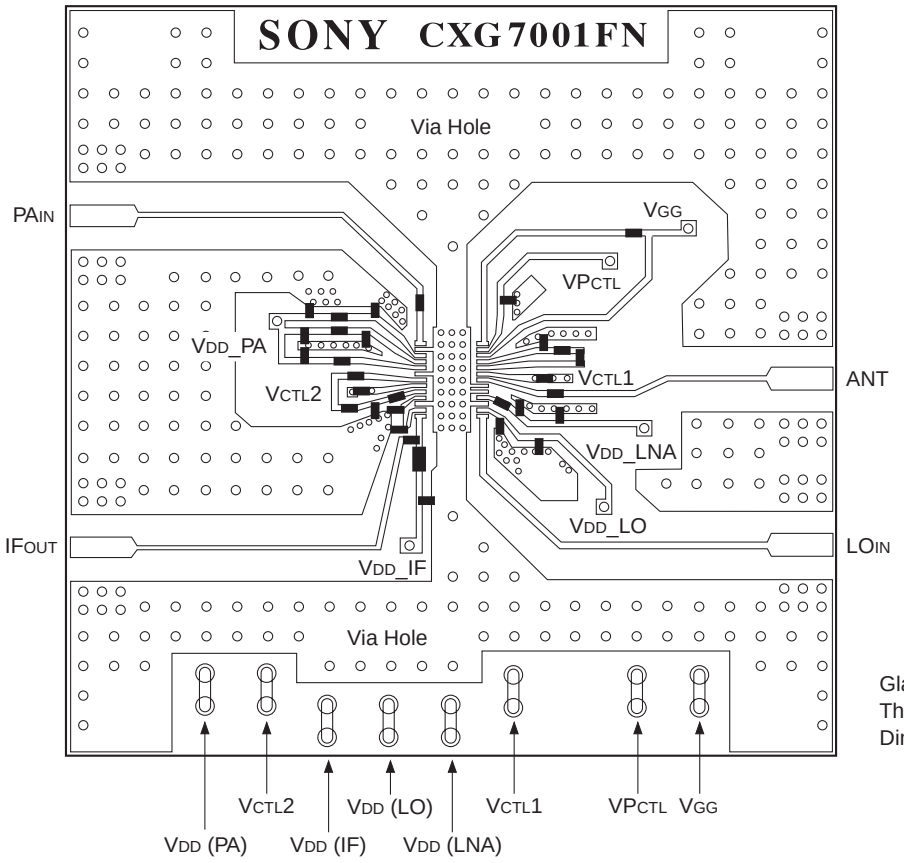


Input IP3, PLK vs. PLO

VDD = 3V, VCTL1 = 0V, VCTL2 = 3V,
RF = 1.90GHz/–35dBm, LO = 1.66GHz

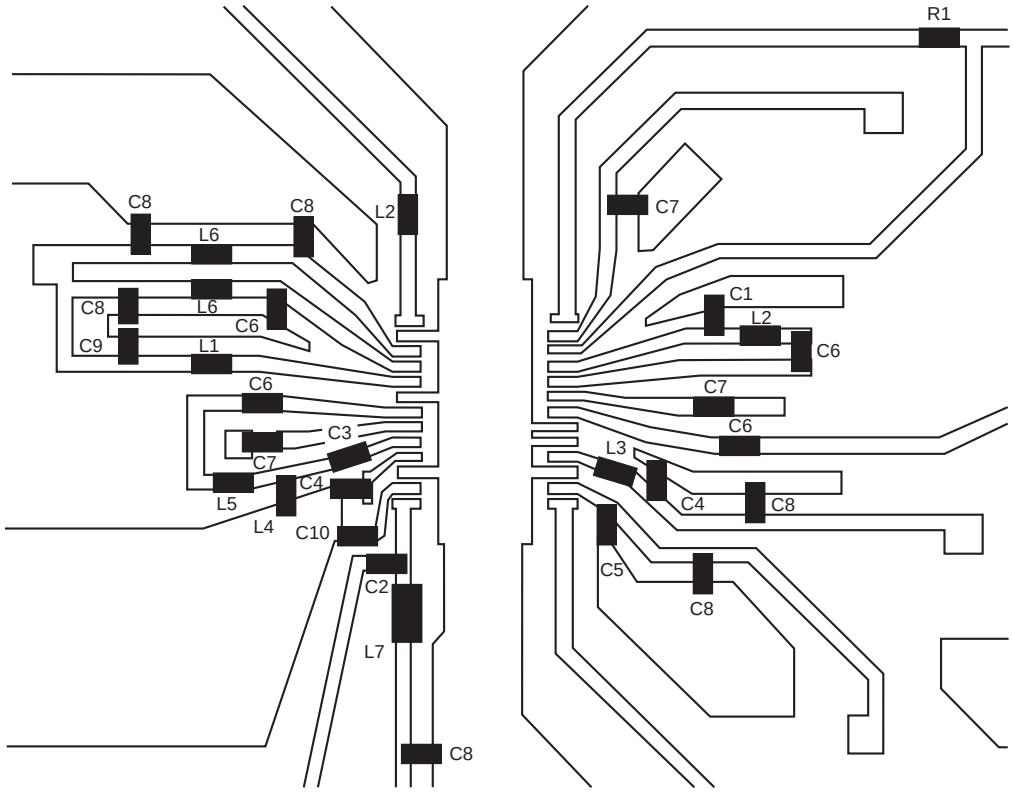


Recommended Evaluation Board



Glass fabric-base epoxy board (4 layers)
Thickness between 1 and 2: 0.2mm
Dimensions: 50mm × 50mm

Enlarged Diagram of External Circuit Block



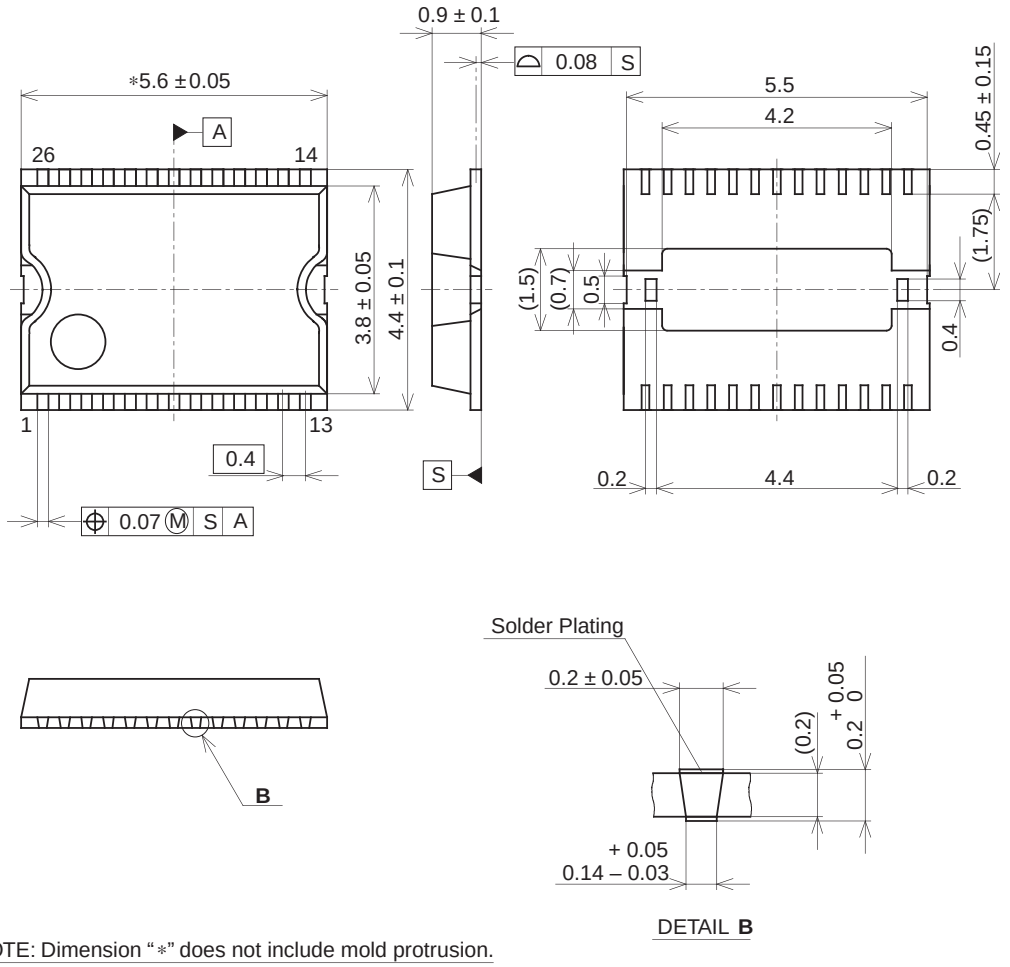
R1 = 1k

L1 = 1.8nH
L2 = 2.2nH
L3 = 3.9nH
L4 = 6.8nH
L5 = 10nH
L6 = 18nH
L7 = 82nH

C1 = 1pF
C2 = 5pF
C3 = 10pF
C4 = 13pF
C5 = 18pF
C6 = 30pF
C7 = 100pF
C8 = 1nF
C9 = 10nF
C10 = 100nF

Package Outline Unit: mm

HSOF 26PIN (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	HSOF-26P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm