

## High Isolation SPDT Switch

### Description

The CXG1009TN is a high Isolation SPDT (Single Pole Dual Throw) switch MMIC for personal communication, cable TV and so on.

This IC is designed using the Sony's GaAs J-FET process and operates at a single positive control supply.

### Features

- Single positive control supply operation
- Insertion Loss
  - 0.7 dB (Typ.) @1.0 GHz,  $V_{ctl} (H)=3\text{ V}$
  - 0.8 dB (Typ.) @2.0 GHz,  $V_{ctl} (H)=3\text{ V}$
- High Isolation
  - 56 dB (Typ.) @1.0 GHz,  $V_{ctl} (H)=3\text{ V}$
  - 47 dB (Typ.) @2.0 GHz,  $V_{ctl} (H)=3\text{ V}$
- 10pin TSSOP package (3.2 × 2.8 mm)

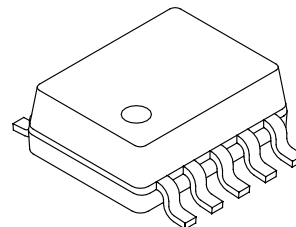
### Applications

- Basestation Lo switching.
- Other Low Power SPDT applications requiring high isolation (e.g. Cable TV).

### Structure

GaAs J-FET MMIC

10 pin TSSOP (Plastic)



### Absolute Maximum Ratings (Ta=25 °C)

- |                         |                             |             |    |
|-------------------------|-----------------------------|-------------|----|
| • Control voltage       | $V_{CTL}$                   | 6           | V  |
|                         | $V_{CTL} (H) - V_{CTL} (L)$ | 6           | V  |
| • Control Current       | $I_{CTL}$                   | 2           | mA |
| • Operating temperature | $T_{opr}$                   | -35 to +85  | °C |
| • Storage temperature   | $T_{stg}$                   | -65 to +150 | °C |

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**Electrical Characteristics**

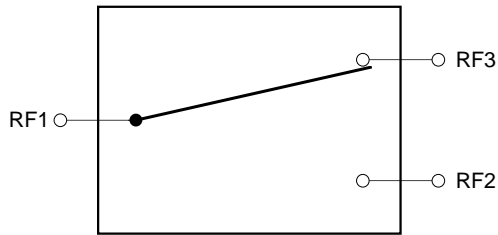
$V_{CTL} (L) = 0\text{ V}$ ,  $V_{CTL} (H) = 3\text{ V}$ ,  $P_{in} = 10\text{ dBm}$

( $T_a = 25\text{ }^\circ\text{C}$ )

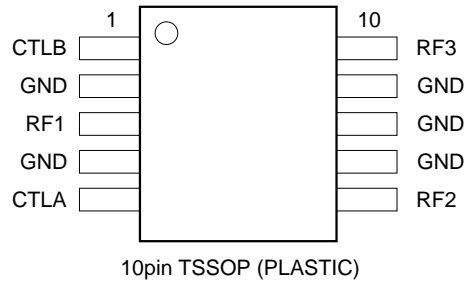
Item	Symbol	Condition	MIN.	TYP.	MAX.	UNit
Insertion Loss 1	IL1	$f \leq 1\text{ GHz}$		0.7	1.1	dB
Isolation 1	ISO1		52	56		dB
Insertion Loss 2	IL2	$f \leq 2\text{ GHz}$		0.8	1.2	dB
Isolation 2	ISO2		43	47		dB
VSWR	VSWR			1.2	1.5	
Switching Speed	TSW			100		ns
Control Current	$I_{CTL}$			60	200	$\mu\text{A}$
1 dB Compression	P1dB	$500\text{ MHz} \leq f \leq 2\text{ GHz}$	16	19		dBm
		$f = 5\text{ MHz}$		8		dBm

50  $\Omega$  source and load impedance

**Block Diagram**

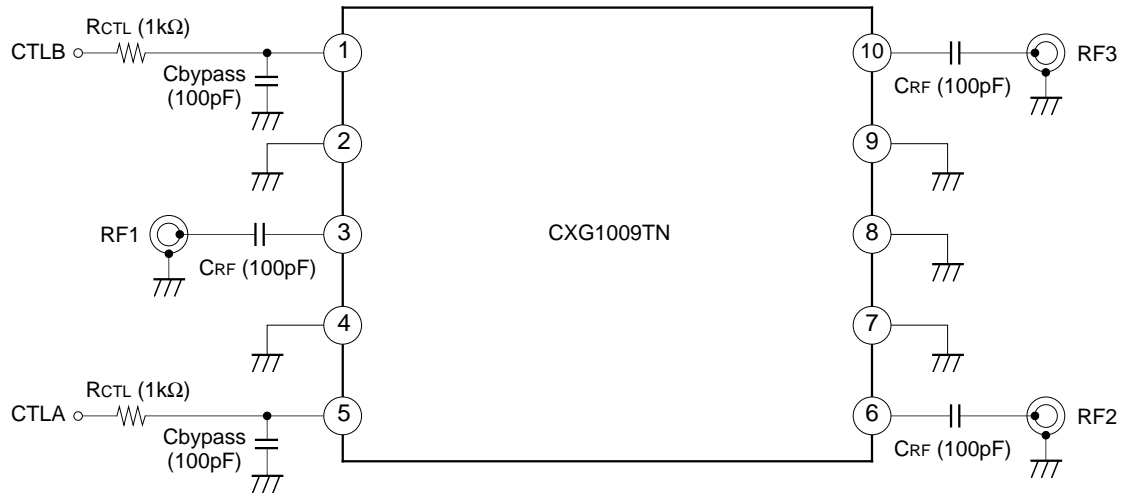


**Package Outline/Pin Configuration**



VCTLA	VCTLB	
High	Low	RF1-RF2 ON RF1-RF3 OFF
Low	High	RF1-RF2 OFF RF1-RF3 ON

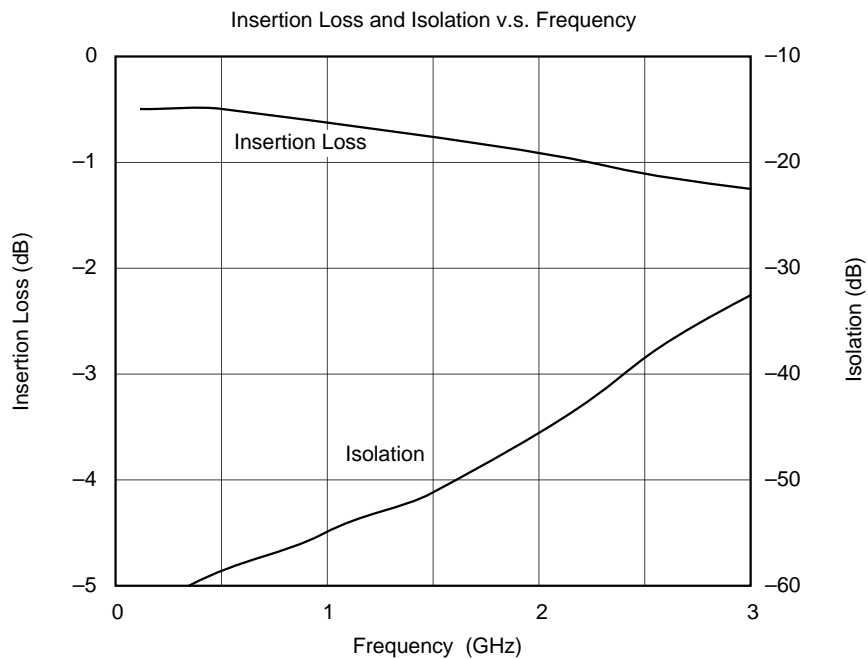
**Recommended Circuit**



- \* It is necessary to use DC blocking capacitors  $C_{RF}$  and bypass capacitors  $C_{bypass}$ .
- \* It is necessary to use control resistors  $R_{CTL}$ , if current consumption needs to be reduced or ESD performance needs to be improved.
- \* It is necessary to operate at low frequency, DC blocking capacitors  $C_{RF}$  needs higher values.

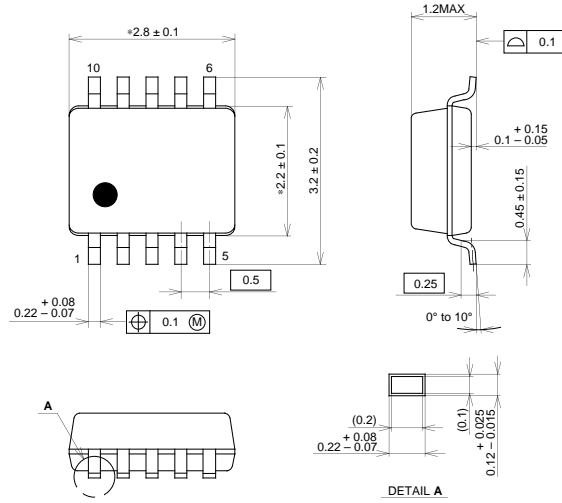
**Frequency characteristics**

Measurement Conditions :  $V_{ctl(L)} = 0\text{ V}$ ,  $V_{ctl(H)} = 3\text{ V}$ ,  $P_{in} = 0\text{ dBm CW}$ ,  $T = 25\text{ °C}$



Package Outline Unit : mm

10PIN TSSOP(PLASTIC)

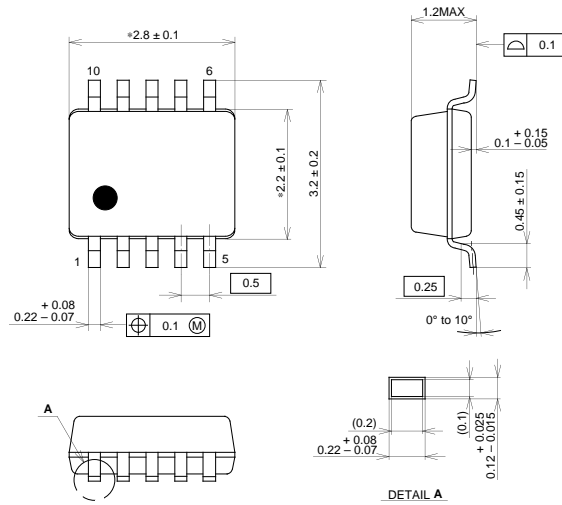


NOTE: Dimension "\*" does not include mold protrusion.

SONY CODE		TSSOP-10P-L01	
EIAJ CODE			
JEDEC CODE			

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

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LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18 $\mu$ m