

CXD2840ER

Description

The CXD2840ER is a DTMB and DVB-C demodulator that conforms to the GB20600-2006 (Terrestrial) and ETSI EN 300-429 (Cable) standards.

It receives signal from the tuner and outputs signal in TS format after demodulation.

Features

General FEATURES

- ◆ All internal clocks derived from signal fixed 41 MHz/20.5 MHz frequency crystal with tolerance up to ± 100 ppm. (Can be shared with CXD2831WR SiTuner or other Sony Analogue/Digital demodulator)
- ◆ High performance differential ADC
- ◆ Fast 400 kHz I²C compatible bus interface
- ◆ Gateway I²C interface for dedicated tuner control
- ◆ Programmable I²C addresses allowing up to four devices to be connected in a single system
- ◆ Automatic IF AGC and optional programmable GPIO interface
- ◆ Configurable parallel and serial MPEG-2 TS outputs with smoothing buffer
- ◆ Built-in de-interleave memory (No external memory required)
- ◆ 3.3 V, 1.2 V power supplies
- ◆ Temperature range -20 to +85 °C
- ◆ 48 pin VQFN 7 mm x 7 mm package (0.5 mm pin pitch)
- ◆ Low operating power consumption (Clear channel)
 - ◆ DTMB C1 : 852 mW (typ.)
 - ◆ DTMB C3780 : 608 mW (typ.)
 - ◆ DVB-C : 207 mW (typ.)
- ◆ Standby mode
 - ◆ Sleep : 52 mW (typ.)
 - ◆ Shutdown : Less than 1 mW (typ.)

Features DTMB

- ◆ Conforms to GB20600-2006
 - ◆ C1 (Single carrier) and C3780 (OFDM)
 - ◆ Frame Header Length: PN420V, PN420C, PN595, PN945V, PN945C
 - ◆ Constellation: 64QAM, 32QAM, 16QAM, 4QAM, 4QAM-NR
 - ◆ Code Rate: 0.4, 0.6, 0.8 (32QAM, 4QAM-NR only support 0.8)
 - ◆ Time Interleave: M720, M240
- ◆ Full compliance with requirements of the GB/T20683,20686-2011 standards
 - ◆ Excellent performance in parameter sets other than the seven modes stipulated by to the GB/T20683,20686-2011 standards
- ◆ Enhanced in the following areas
 - ◆ Improved dynamic multipath performance
 - ◆ Improved pre-echo performance
 - ◆ Improved performance for impulsive noise
- ◆ Outstanding Adjacent Channel Interference tolerance
- ◆ Outstanding channel scanning performance through rejection of non-digital signals

Features DVB-C

- ◆ Conforms to ETSI EN 300-429
 - ◆ Modulation: 16QAM, 32QAM, 64QAM, 128QAM, 256QAM
 - ◆ Symbol Rate: 0.7 to 7.2 Msym/s
- ◆ Complies with NorDig-Unified Ver2.2
- ◆ Wide symbol range, 1.8 to 7.2Msym/s
- ◆ Integrated matched filter 0.15 roll-off factor
- ◆ Frequency offset detection range up to ± 500 kHz allows acquisition and performance optimization via tuner frequency offset compensation
- ◆ Enhanced in the following areas
 - ◆ Improved equalization for cancellation of reflections at larger delays
 - ◆ Improved accuracy on symbol rate and SNR monitor
- ◆ Outstanding channel scanning performance through rejection of non-digital signals

APPLICATIONS

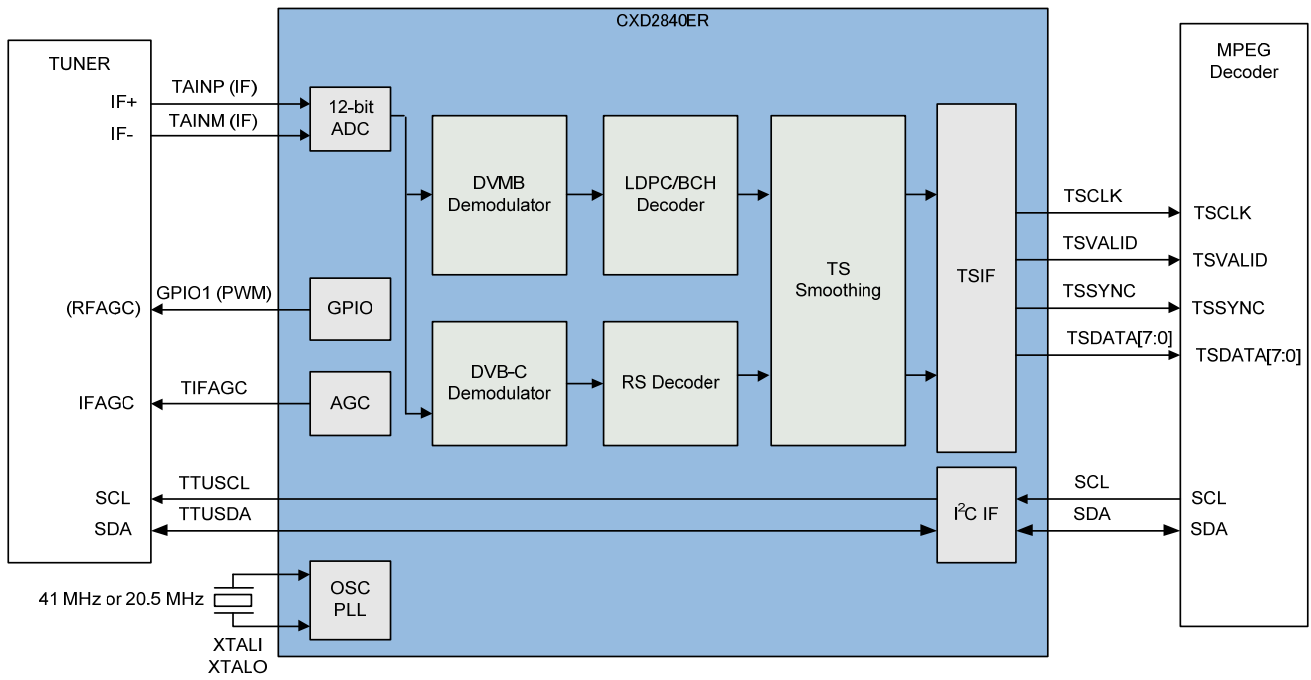
- ◆ Set Top Boxes
- ◆ IDTV with Digital only or Hybrid Tuner Support
- ◆ PC TV
- ◆ PVRs and recordable Blu-rayTM/DVD players
- ◆ Professional equipment

Contents

Description	1
Features	1
General FEATURES	1
Features DTMB	2
APPLICATIONS	2
1. Block Diagram	5
2. Pin Configuration	6
3. Absolute Maximum Ratings	7
4. Recommended Operating Conditions	8
5. DC Electrical Characteristics	9
6. AC Electrical Characteristics	11
6.1. I ² C Interface	11
6.2. IF Input Interface	12
6.3. Clock Input Interface	12
6.4. GPIO Interface	12
6.5. Reset Interface	13
6.6. I ² C Repeater Interface	13
6.7. AGC Output Interface	13
6.8. TS Output Interface	14
6.9. Other Input Interfaces	14
7. Power Supply Sequence	15
8. Pin Description	16
9. I/O Interfaces	19
9.1. Clock Input Interface	19
XTALI, XTALO	19
OSCEN_X	19
9.2. IF Input Interface	20
TAINP, TAINM	20
9.3. Hardware Reset	20
RST_X	21
9.4. I ² C Interface	22
9.4.1. Host I ² C Sequence	24
9.4.2. I ² C Gateway Sequence	25
9.5. AGC Output Interface	26
TIFAGC	26
GPIO1 (PWM)	26
9.6. TS Output Interface	27
TSCLK, TSVALID, TSSYNC, and TSDATA[7:0]	27

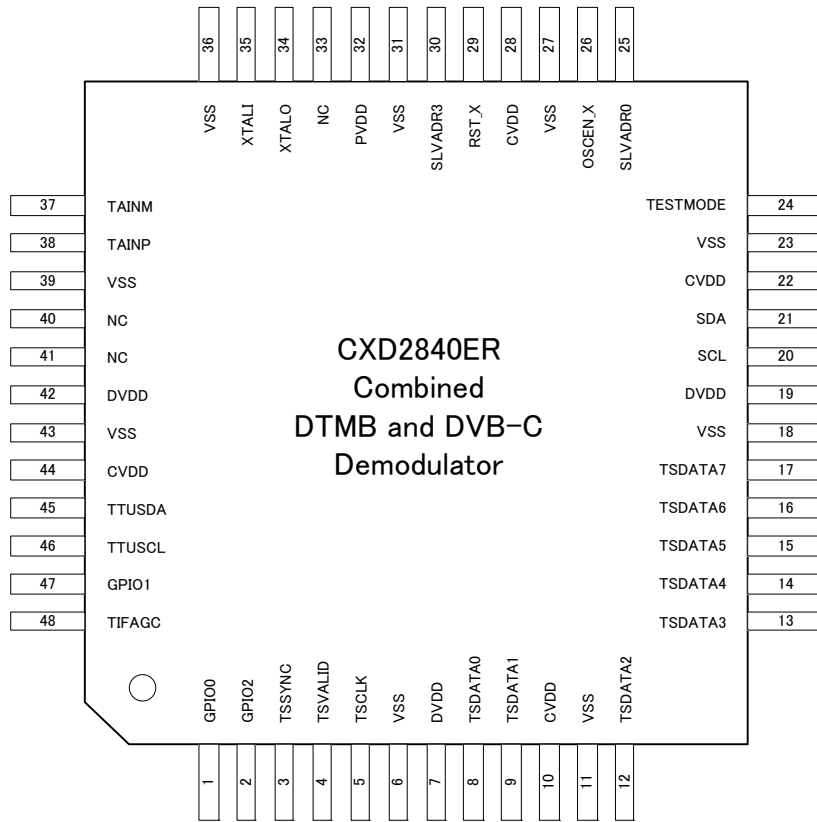
9.7. General Purpose I/O -----	27
GPIO0, GPIO1, GPIO2-----	27
9.8. Test pins-----	28
TESTMODE-----	28
10. Package Outline -----	29
11. Marking-----	30

1. Block Diagram



2. Pin Configuration

(Top View)



3. Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

(Ta = 25 °C, VSS = 0 V)

Item	Symbol	Rating (*1)	Unit
Power Supplies	CVDD	-0.3~+1.68	V
	DVDD	-0.3~+4.62	V
	PVDD	-0.3~+1.68	V
Input Voltage	V _{IN}	-0.3 to VDD33+0.3 (4.62 max.) (*6)	V
	V _{IN5} (*2)	-0.3 to VDD33+3.6 (6.00 max.) (*5, *6)	V
	V _{INI2C} (*3)	-0.5 to VDD33+3.6 (6.00 max.) (*5, *6)	V
	V _{IN25} (*4)	-0.3 to VDD25+0.3 (3.5 max.) (*7)	V
Storage Temperature	Tstg	-65~+150	°C

*1 Absolute maximum rating values must not be exceeded, even momentarily, for any item. In addition, even when the absolute maximum ratings and operating range are not exceeded, use of this product under operating conditions (operating temperature, current, voltage, etc.) that apply a continuously high load (high temperature with high current and high voltage applied, large temperature changes, etc.) may significantly degrade reliability.

*2 V_{IN5} is the 5 V tolerant I/O rating. The applicable pins are RST_X, OSCEN_X, SLVADR0, TTUSCL, TTUSDA, SLVADR3, GPIO0, GPIO1, GPIO2, and TESTMODE.

*3 V_{INI2C} is the I2C input rating. The applicable pins are SCL and SDA.

*4 V_{IN25} is the analog input rating. The applicable pins are TAINM, TAINP and XTALI.

*5 5 V tolerant inputs are only 5 V tolerant while the CXD2840ER power is applied. If no power is applied to CXD2840ER there is no protection to 5 V levels and the CXD2840ER may be permanently damaged. It is important to observe the conditions for 5 V protection when sequencing power supplies in the application.

*6 VDD33 is DVDD

*7 VDD25 is internally regulated voltage. When the CXD2834 is powered-on, the ADC and internal regulator are disabled and VDD25 = 0 V. After the ADC and internal regulator are enabled by register setting, VDD25 = 2.3 V.

4. Recommended Operating Conditions

Table 2: Recommended Operating Conditions

($T_a = 25\text{ }^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supplies	CVDD	1.08	1.2	1.32	V
	DVDD	3.0	3.3	3.6	V
	PVDD	1.08	1.2	1.32	V
Input Voltage	V_{IN}	—	—	DVDD+0.3 (3.6 max.)	V
	V_{IN5} (*1)	—	—	DVDD+2.5 (5.5 max.)	V
	V_{INI2C} (*2)	—	—	DVDD+2.5 (5.5 max.)	V
Output Voltage	V_{OUT}	0	—	3.6	V
Junction Temperature	T_j	-20	—	+125	$^\circ\text{C}$
Ambient Temperature	T_a	-20	—	+85	$^\circ\text{C}$

*1 V_{IN5} is the 5 V tolerant I/O rating. The applicable pins are RST_X, OSCEN_X, SLVADR0, SLVADR3, TTUSCL, TTUSDA, GPIO0, GPIO1, GPIO2, and TESTMODE.

*2 V_{INI2C} is the I2C input rating. The applicable pins are SCL and SDA.

*3 To ensure exact and reliable operation, the CXD2840ER should operate within the range of the recommended operating conditions.

*4 Design CVDD power supply circuit very carefully within recommended operation range because operation current changes widely during DTMB reception.

*5 The voltage must not be supplied partially to CVDD, DVDD and PVDD.

5. DC Electrical Characteristics

Table 3: DC Electrical Characteristics

(VSS = 0 V, supply voltage and temperature within the recommended operating conditions)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pins
Input High Voltage	V _{IH}	—	2.0	—	DVDD+0.3 (3.6 max.)	V	—
	V _{IH5}	—	2.0	—	DVDD+2.5 (5.5 max.)	V	(b), (c), (d), (e)
Input Low Voltage	V _{IL}	—	-0.3	—	0.8	V	(b), (c), (d), (e)
I ² C Bus Voltage	V _{BUSI2C}	—	2.97	3.3	5.0	V	—
I ² C Input High Voltage	V _{IHI2C}	—	V _{BUSI2C} *0.7	V _{BUSI2C}	V _{BUSI2C} +0.5	V	(a)
I ² C Input Low Voltage	V _{ILI2C}	—	-0.5	0.0	V _{BUSI2C} *0.3	V	(a)
Output High Voltage (*1)	V _{OH2}	I _O = 2 mA	DVDD-0.4 V	3.3	—	V	TIFAGC
	V _{OH4}	I _O = 4 mA	DVDD-0.4 V	3.3	—	V	—
	V _{OH8}	I _O = 8 mA	DVDD-0.4 V	3.3	—	V	(d), (f)
	V _{OH10}	I _O = 10 mA	DVDD-0.4 V	3.3	—	V	(f)
Output Low Voltage (*1)	V _{OL2}	I _O = 2 mA	—	0.0	0.4	V	TIFAGC
	V _{OL4}	I _O = 4 mA	—	0.0	0.4	V	TTUSDA, TTUSCL
	V _{OL8}	I _O = 8 mA	—	0.0	0.4	V	(d), (f)
	V _{OL10}	I _O = 10 mA	—	0.0	0.4	V	(f)
	V _{OLSDA}	I _O = 3 mA	—	0.0	0.4	V	SDA
Input High Current	I _{IH}	V _I = DVDD	—	—	±10	μA	—
	I _{IH5}	V _I = 5.5 V	—	—	±10	μA	(a), (b), (c), (d), (e)
Input Low Current	I _{IL}	V _I = 0 V	—	—	±10	μA	(a), (b), (c), (d), (e)
Output Leakage Current	I _{OZ}	V _O = DVDD or 0 V	—	—	±10	μA	(d), (f), TIFAGC
	I _{OZSDA}	V _O = 5.5 V or 0 V	—	—	±10	μA	SDA
Input Pull-up Resistor (*2)	R _{PU}	—	26	38	60	kΩ	(c), (d), (f)
Input Pull-down Resistor	R _{PD}	—	33	47	81	kΩ	(b)
Power-off Leakage Current	I _{OFF}	DVDD = 0 V V _I = 3.6 V or 0 V	—	—	±10	μA	(a), (b), (c), (d), (e)
IF Input Dynamic Range	V _{IIF}	TAINP-TAINM Selectable by register	1.4, 1.0, 0.7			Vp-p	TAINP, TAINM
XTALI Input Dynamic Range	V _{IXI}	AC coupled sine wave	0.35	—	1.0	Vp-p	XTALI
XTALO Transconductance	gm	Δ of I _O = -2 mA and I _O = 0 mA	14.4	—	28.5	mS	XTALO
XTALI DC BIAS Voltage	V _{BIASXI}	—	0.6	0.8	1.0	V	XTALI
Operating Current DTMB C1 operation (Max Operating Current)	IDVDD (*3)	Measurement condition: 64QAM, PN595, P_off, Rate0.8, IL720, Multipath, CNR=20dB	—	46.2	64.1	mA	DVDD
	ICVDD		—	702	817	mA	CVDD
	IPVDD		—	0.5	0.6	mA	PVDD
Operating Current DTMB C1 operation	IDVDD (*3)	Measurement condition: 16QAM, PN595, P_off, Rate0.8, IL240, CNR=12.6dB	—	46.2	64.1	mA	DVDD
	ICVDD		—	582	682	mA	CVDD
	IPVDD		—	0.5	0.6	mA	PVDD

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pins
Operating Current DTMB C3780 operation	IDVDD (*3)	Measurement condition: 16QAM, PN945V, Rate0.6, IL240, CNR=13.2dB	—	46.2	64.1	mA	DVDD
	ICVDD		—	379	482	mA	CVDD
	IPVDD		—	0.5	0.6	mA	PVDD
Operating Current DVB-C operation	IDVDD (*3)	Measurement condition: 7.0Msym/s, 256QAM, CNR=32dB	—	46.2	64.1	mA	DVDD
	ICVDD		—	44.6	71.0	mA	CVDD
	IPVDD		—	0.5	0.6	mA	PVDD
Standby Current Sleep mode	IDVDD (*3)	When in Sleep Mode	—	13.2	17.1	mA	DVDD
	ICVDD		—	6.1	12.5	mA	CVDD
	IPVDD		—	0.5	0.6	mA	PVDD
Standby Current Shutdown mode	IDVDD (*3)	When in Shutdown Mode	—	6.7	11.0	μA	DVDD
	ICVDD		—	0.7	7.6	mA	CVDD
	IPVDD		—	2.3	6.0	μA	PVDD

(a): SCL, SDA

(b): TESTMODE, SLVADR0

(c): OSCEN_X, SLVADR3

(d): GPIO0, GPIO2, GPIO1

(e): RST_X, TTUSDA, TTUSCL

(f): TSCLK, TSSYNC, TSVALID, TSDATA[7:0]

*1 Output current of (f) group can be changed by the register settings.

*2 Pull-up resistance of (d) and (f) group can be enabled or disabled by the register settings.

*3 DVDD current consumption is calculated based on the following assumptions:

Typical Current: TS loading 15 pF, TIFAGC loading 1 pF held at center voltage, only OSCEN_X internal pull-up resistor driven by the opposite polarity, GPIO1 is not active.

Maximum Current: TS loading 15 pF, TIFAGC/ GPIO1 loading 15 pF held at center voltage, all internal pull-up/down resistor driven by the opposite polarity. GPIO1 as PWM is active.

6. AC Electrical Characteristics

(VSS = 0 V, supply voltage and temperature within the recommended operating conditions)

6.1. I²C Interface

Corresponding I/O names are: SCL, SDA

Table 4: AC Electrical Characteristics of I²C Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f _{SCL}	Fast Mode Standard Mode		400 100		kHz
Hold time START condition	t _{HD:STA}		0.6	—	—	μs
Low period of the SCL clock	t _{LOW}		1.3	—	—	μs
High period of the SCL clock	t _{HIGH}		0.6	—	—	μs
Setup time for a repeated START condition	t _{SU:STA}		0.6	—	—	μs
Data hold time	t _{HD:DAT}		0.0	—	0.9	μs
Data setup time	t _{SU:DAT}		100	—	—	ns
Setup time for STOP condition	t _{SU:STO}		0.6	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		1.3	—	—	μs
Output fall time	t _{of}	*1	21	—	250	ns
Output rise time	t _{or}	*2	21	—	300	ns
Pulse width of spikes allowed	t _{SP}		—	—	50	ns
Input capacitance	C _{IN}		—	—	13.4	pF
Output load capacitance	C _{LD}		—	—	400	pF

*1 Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF.

*2 Output rise time from V_{ILmax} to V_{IHmin} with a bus capacitance from 10 pF to 400 pF.

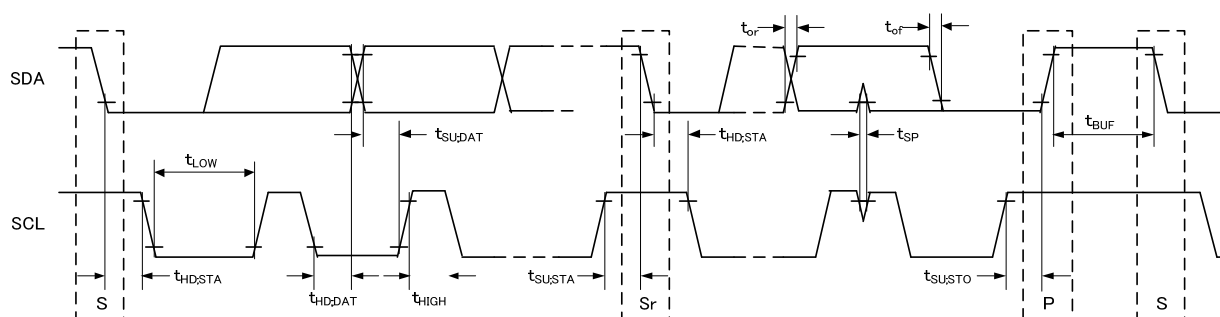


Fig. 1. Waveform of I²C Interface

6.2. IF Input Interface

Corresponding I/O names are: TAINP, TAINM

Table 5: AC Electrical Characteristics of IF Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input bandwidth	F_{IN}	Fosc = 41 MHz or 20.5 MHz	0.5	—	60	MHz
Input impedance	Z_{diff}	Fosc = 41 MHz or 20.5 MHz	1.9	—	2.6	k Ω
	Z_{com}	ADCEN = 1	1.2	—	1.8	k Ω
Input capacitance	C_{IN}	CLKGENEN = 1 AREGEN = 1 *1	4.1	—	8.5	pF
Input impedance in Sleep Mode	$Z_{diffSLEEP}$	ADCEN = 0	2.5	—	3.8	k Ω
	$Z_{comSLEEP}$	CLKGENEN = 0	3.1	—	4.4	k Ω
Input capacitance in Sleep Mode	$C_{INSLEEP}$	AREGEN = 0 *2	1.3	—	4.8	pF

*1 ADCEN, CLKGENEN and AREGEN are the register settings of ADC that enables ADC.

ADCEN = 1, CLKGENEN = 1 and AREGEN = 1 when the ADC is active.

*2 DC bias is disabled when the internally regulated 1.2 V is turned off by setting ADCEN = 0 and AREGEN = 0.

Thus TAINP and TAINM pins are pulled at 0 V in DC. In this state and depending on the voltage level, any analogue input signal may be clamped to VSS by the ESD device.

6.3. Clock Input Interface

Corresponding I/O names are: XTALI, XTALO

Mode of operation: FUNDAMENTAL

Table 6: AC Electrical Characteristics of Clock Input Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input clock frequency	F_{OSC}		—	41 or 20.5 *1	—	MHz
Accuracy	F_{tol}	*2	—	—	±100	ppm
Input impedance	Z_{IN}	Applies to XTALI	170	—	230	k Ω
Input capacitance	C_{IN}	Applies to XTALI	3.2	—	7.2	pF
Output capacitance	C_{OUT}	Applies to XTALO	1.0	—	4.3	pF

*1 Register setting is necessary for 20.5 MHz

*2 Total of Frequency tolerance, aging and temperature stability

6.4. GPIO Interface

Corresponding I/O names are: GPIO0, GPIO1, and GPIO2

Table 7: AC Electrical Characteristics of GPIO Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}		—	—	6.7	pF
Output load capacitance	C_{LD}		—	—	20	pF

6.5. Reset Interface

Corresponding I/O name is: RST_X

Table 8: AC Electrical Characteristics of Reset Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}		—	—	6.8	pF

6.6. I²C Repeater Interface

Corresponding I/O names are: TTUSCL, TTUSDA

The I²C Repeater Interface supports the mandatory protocol features for a Single master configuration as listed in the NXP specification reference document: UM10204 "I²C-Bus specification and user manual Rev. 03 – 19 June 2007". Refer to Table 2 on page 8 of the reference document.

Table 9: AC Electrical Characteristics of I²C Repeater Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}		—	—	6.8	pF
Output load capacitance	C _{LD}		—	—	20	pF

6.7. AGC Output Interface

Corresponding I/O names are: TIFAGC, GPIO1

Table 10: AC Electrical Characteristics of AGC Output Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output load capacitance *1	C _{LPWM}		—	—	15	pF

*1 Output load capacitance value is the allowable capacitance value until the RC filter.

6.8. TS Output Interface

Corresponding I/O names are: TSCLK, TSVALID, TSSYNC, TSDATA[7:0]

TSVALID, TSSYNC and TSDATA[7:0] are triggered by TSCLK negative edge in default.

TSCLK may be inverted by register.

Table 11: AC Electrical Characteristics of TS Output Interface of DTMB

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TS clock cycle	$t_{CYC;S}$	TS Serial	12.1	—	—	ns
	$t_{CYC;P}$	TS Parallel	243.9	—	—	ns
TS clock low period	$t_{LOW;S}$	TS Serial	5.4	—	—	ns
	$t_{LOW;P}$	TS Parallel	121.3	—	—	ns
TS clock high period	$t_{HIGH;S}$	TS Serial	5.4	—	—	ns
	$t_{HIGH;P}$	TS Parallel	121.3	—	—	ns
Propagation delay	$t_{PD;S}$	TS Serial	-2.4	—	1.9	ns
	$t_{PD;P}$	TS Parallel	-2.4	—	2.4	ns
Output load capacitance	C_L	$I_{OH} = 8 \text{ mA}$	—	—	15	pF

Table 12 AC Electrical Characteristics of TS Output Interface of DVB-C

Item	Symbol	Condition	Min	Typ	Max	Unit
TS clock cycle	$t_{CYC;S}$	TS Serial	12.1	—	—	ns
	$t_{CYC;P}$	TS Parallel	146.3	—	—	ns
TS clock low period	$t_{LOW;S}$	TS Serial	5.4	—	—	ns
	$t_{LOW;P}$	TS Parallel	72.5	—	—	ns
TS clock high period	$t_{HIGH;S}$	TS Serial	5.4	—	—	ns
	$t_{HIGH;P}$	TS Parallel	72.5	—	—	ns
Propagation delay	$t_{PD;S}$	TS Serial	-2.4	—	1.9	ns
	$t_{PD;P}$	TS Parallel	-2.4	—	2.4	ns
Output load capacitance	CL8	$I_{OH}=8\text{mA}$	—	—	15	pF

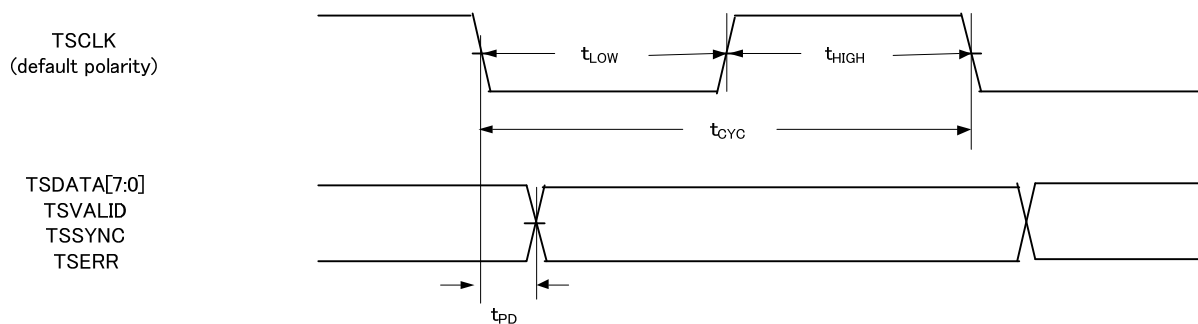


Fig. 2. Waveform of TS Output Interface

6.9. Other Input Interfaces

Corresponding I/O names are: TESTMODE, SLVADR0, SLVADR3, and OSCEN_X

Table 13: AC Electrical Characteristics of Other Interfaces

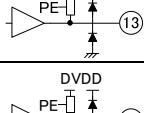
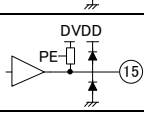
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}		—	—	6.8	pF

7. Power Supply Sequence

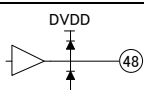
For all power supplies (i.e. CVDD, DVDD, and PVDD), there is no restriction on the order of applying or removing the power supplies.

8. Pin Description

Table 14: Pin Description

Pin No.	Symbol	I/O	Function	Equivalent Circuit	Note
1	GPIO0	I/O	General purpose I/O		5 V tolerant Controllable pull-up
2	GPIO2	I/O	TS error flag General purpose I/O		5 V tolerant Controllable pull-up
3	TSSYNC	O	TS sync flag		Controllable pull-up Selectable output current
4	TSVALID	O	TS valid flag		Controllable pull-up Selectable output current
5	TSCLK	O	TS clock output		Controllable pull-up Selectable output current
6	VSS	—	Ground	n/a	
7	DVDD	—	3.3 V power supply	n/a	
8	TSDATA0	O	TS data output		Controllable pull-up Selectable output current
9	TSDATA1	O	TS data output		Controllable pull-up Selectable output current
10	CVDD	—	1.2 V power supply	n/a	
11	VSS	—	Ground	n/a	
12	TSDATA2	O	TS data output		Controllable pull-up Selectable output current
13	TSDATA3	O	TS data output		Controllable pull-up Selectable output current
14	TSDATA4	O	TS data output		Controllable pull-up Selectable output current
15	TSDATA5	O	TS data output		Controllable pull-up Selectable output current
16	TSDATA6	O	TS data output		Controllable pull-up Selectable output current
17	TSDATA7	O	TS data output		Controllable pull-up Selectable output current
18	VSS	—	Ground	n/a	
19	DVDD	—	3.3 V power supply	n/a	
20	SCL	I	I ² C clock		5 V tolerant

Pin No.	Symbol	I/O	Function	Equivalent Circuit	Note
21	SDA	I/O	I ² C data		5 V tolerant
22	CVDD	—	1.2 V power supply	n/a	
23	VSS	—	Ground	n/a	
24	TESTMODE	I	Test mode setting		5 V tolerant 1: Test mode 0: Normal mode
25	SLVADR0	I	I ² C slave address selection		5 V tolerant
26	OSCEN_X	I	Oscillator enable		5 V tolerant 1: Stop 0: Run
27	VSS	—	Ground	n/a	
28	CVDD	—	1.2 V power supply	n/a	
29	RST_X	I	Hardware reset		5 V tolerant
30	SLVADR3	I	I ² C slave address selection		5 V tolerant
31	VSS	—	Ground	n/a	
32	PVDD	—	1.2 V power supply	n/a	Supplies PLL power
33	NC	—	—	n/a	
34	XTALO	O	Crystal oscillator output		Leave open when external clock input to XTALI
35	XTALI	I	Crystal oscillator input		External clock input pin
36	VSS	—	Ground	n/a	
37	TAINM	I	IF input (-)		
38	TAINP	I	IF input (+)		
39	VSS	—	Ground	n/a	
40	NC	—	—	n/a	
41	NC	—	—	n/a	
42	DVDD	—	3.3 V power supply	n/a	
43	VSS	—	Ground	n/a	
44	CVDD	—	1.2 V power supply	n/a	
45	TTUSDA	I/O	Tuner I ² C data		5 V tolerant
46	TTUSCL	O	Tuner I ² C clock		5 V tolerant
47	GPIO1	I/O	RFAGC output General purpose I/O		PWM output 5 V tolerant Controllable pull-up CAUTION: intermediate voltage input is prohibited.

Pin No.	Symbol	I/O	Function	Equivalent Circuit	Note
48	TIFAGC	O	TIFAGC output		PWM output CAUTION: 5 V input is prohibited.

*1 Input voltage up to 3.6 V is acceptable on 5 V tolerant inputs even when the CXD2840ER power is off. Do not apply voltage on non 5 V tolerant inputs when the CXD2840ER power is off.

*2 The following list shows the pins that may be unused depending on application. The following list is the directions of how the unused pins are terminated to keep stable operation of the device.

*3 These are internally regulated voltages When the CXD2834 is powered-on, ADC and internal regulator are disabled and VDD25/VDD12=0 V. After ADC and internal regulator are enabled by register setting, VDD25=2.5 V and VDD12=1.2 V.

Table 15: How to terminate unused pins

Pin Names	Direction
XTALO	Leave pin open when external clock supplied to XTALI. Avoid any extra loading to XTALO that may obstruct the clock propagation from XTALI to the core.
TSSYNC, TSVALID, TSCLK, TSDATA7-0 TIFAGC	These pins may be left open.
GPIO0, GPIO1, GPIO2	These pins may leave open, but make sure the internal pull-up is enabled.
TTUSCL, TTUSDA	Pull-up the pins as the same way using I ² C.

9. I/O Interfaces

9.1. Clock Input Interface

Corresponding I/O names are: XTALI, XTALO, OSCEN_X

The CXD2840ER operates with the clock reference from a crystal or external clock source input. XTALI and XTALO are the crystal oscillator interface of the internal oscillator. OSCEN_X is the control signal for the oscillator. With these pins, users can control the reference clock of the demodulator.

XTALI, XTALO

Internal voltage bias: Exists on XTALI.

There are two ways to input clock, one is to connect crystal, and other is to input external clock source to XTALI. No register settings are required for clock source selection.

OSCEN_X

I/O type: Pull-up, 5 V tolerant

This enables or disables the crystal oscillator. Set OSCEN_X to 0 to enable the oscillator. The pin is internally pulled-up. Therefore, when the pin is open, OSCEN_X becomes 1 and the oscillator be disabled.

The oscillator uses the internal bias voltage to pull XTALI to the threshold level of the internal circuit. When there is no clock applied to XTALI, the level of XTALI is close to the threshold level of the parasitic noise and there is a risk of hazardous clock propagation to the internal logic. To avoid this hazardous situation, it is recommended that OSCEN_X is set to 1 when there is no clock supplied to XTALI.

The level of OSCEN_X must be set before hardware reset is negated.

Table 15: OSCEN_X truth table

OSCEN_X	Description
0	Enable oscillator. The oscillator generates clock when 41 MHz or 20.5 MHz crystal is connected to XTALI and XTALO. The oscillator propagate clock when 41 MHz or 20.5 MHz external clock is supplied to XTALI.
1	Disable oscillator. Set OSCEN_X to 1 when no external clock is supplied.

9.2. IF Input Interface

Corresponding I/O names are: TAINP and TAINM

TAINP, TAINM

Internal voltage bias exists on both TAINP and TAINM

Initial condition: Sleep mode

These are the differential IF input interfaces.

Standard IF signals and Low IF signals are supported. Low IF signal frequencies are not standardized and restrictions may apply to certain combinations of center frequency and bandwidth.

Table 16: Supported IF center frequency

	IF center frequency
DTMB	High IF frequency: 36 MHz.
DVB-C	Low IF frequency: Typically 4-5 MHz, but other values are possible, please contact local support.

The ADC is internally biased at the center of the dynamic range, so the IF inputs must be AC coupled for the best performance. When the CXD2840ER is powered-up, the CXD2840ER is in sleep mode and the internal bias is disabled. Therefore, the AC signal input may be clamped by the ESD device to ground in sleep mode depending on the voltage level applied.

9.3. Hardware Reset

Corresponding I/O name is: RST_X

The CXD2840ER has 2 types of reset.

Table 17: Reset Types

Reset Type	Description
Hardware Reset	Hardware Rest resets the entire system by RST_X pin.
Software Reset	Software Reset is the I2C register to clear all the system but I ² C registers.

The following explains Hardware Reset.

RST_X

I/O type: Schmitt, 5 V tolerant

This is the Hardware Reset pin to reset the entire CXD2840ER.

The RST_X should be held low for 3 ms after the power supplies have stabilized, to allow the oscillator to stabilize.

A Hardware Reset is also required, before normal operation can be resumed, after the crystal oscillator has been disabled and re-enabled.

Table 18: RST_X truth table

RST_X	Description
0	Assert Hardware Reset
1	Negate Hardware Reset

The following pins; OSCEN_X, SLVADR0, SLVADR3 and TESTMODE must be asserted or negated while RST_X is 0. The only exception is OSCEN_X, the oscillator can be disabled by setting OSCEN_X to 1 while RST_X is 1.

◆When Power On

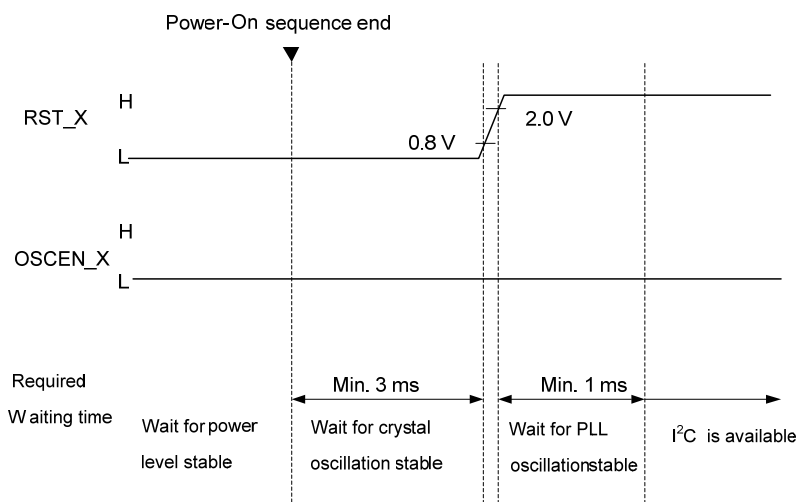


Fig.3. Reset Sequence when Power On

◆When Start up Crystal Oscillation (When changing OSCEN_X from High to Low)

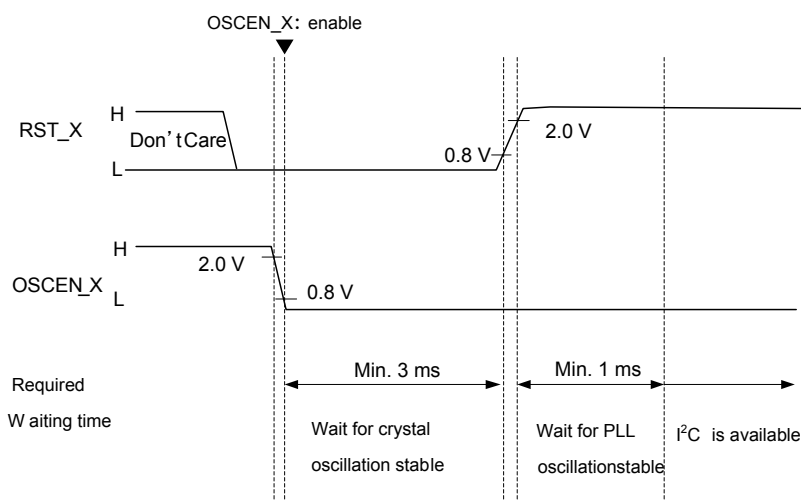


Fig.4. Reset Sequence when Start up Crystal Oscillation

9.4. I²C Interface

Corresponding I/O names are: SCL, SDA, TTUSCL, TTUSDA, SLVADR0 and SLVADR3

I²C bus is used to control the demodulator.

CXD2840ER supports both standard mode and fast mode.

CXD2840ER does not change the mode between host and RF tuner, so whatever mode is selected by the host to communicate with the CXD2840ER is the mode used between CXD2840ER and RF tuner. For example, if the host communicates with the CXD2840ER in Standard Mode using SCL & SDA, the communications between CXD2840ER and RF tuner, using TTUSCL and TTUSDA are also in Standard Mode.

Table 20: I²C modes

I ² C Mode	Description
Standard Mode	SCL operates at 100 kHz. When in standard mode, TTUSCL also operates at 100 kHz.
Fast Mode	SCL operates at 400 kHz. When in fast mode, TTUSCL also operates at 400 kHz.

I²C-bus specification compatibility

The host I²C interface (i.e. SCL and SDA) supports the mandatory protocol features for a Slave configuration as listed in the NXP specification reference document: UM10204 "I²C-Bus specification and user manual Rev. 03 – 19 June 2007".

Refer to Table2 on page 8 of the reference document.

The tuner I²C interface does not support multi-master function.

Access to tuner device

A user accesses to the tuner I²C interface using the I²C gateway function that the CXD2840ER supports.

I²C slave addresses

CXD2840ER uses a 7-bit slave address. The slave address is chosen by setting the SLVADR0 and SLVADR3 pins.

The I²C registers of the DTMB and DVB-C functions share the same slave address, while the oscillator has its own slave address to change the clock frequency between 41 MHz and 20.5 MHz.

Table 21: I²C slave addresses including read/write bit

	When SLVADR0 = 0 and SLVADR3 = 0		When SLVADR0 = 1 and SLVADR3 = 0	
	Write	Read	Write	Read
System DTMB DVB-C	0xC8	0xC9	0xCA	0xCB
Oscillator	0xCC	0xCD	0xCE	0xCF

	When SLVADR0 = 0 and SLVADR3 = 1		When SLVADR0 = 1 and SLVADR3 = 1	
	Write	Read	Write	Read
System DTMB DVB-C	0xD8	0xD9	0xDA	0xDB
Oscillator	0xDC	0xDD	0xDE	0xDF

SCL, SDA

I/O type: Schmitt, 5 V tolerant, Open-drain

Initial condition: Hi-Z

These are I²C slave interface to control the CXD2840ER.

The bus can also control TTUSCL and TTUSDA through the gateway function.

Mandatory protocol features for a Slave configuration are supported as listed in the NXP specification reference document: UM10204 "I²C-Bus specification and user manual Rev. 03 – 19 June 2007". Refer to Table 2 on page 8 of the reference document.

TTUSCL, TTUSDA

I/O type: Schmitt, 5 V tolerant, Open-drain

Initial condition: Hi-Z

These are the I²C repeater bus that connects the CXD2840ER to RF tuner.

The I²C Repeater Interface supports the mandatory protocol features for a Single master configuration as listed in the NXP specification reference document: UM10204 "I²C-Bus specification and user manual Rev. 03 – 19 June 2007". Refer to Table 2 on page 8 of the reference document.

SLVADR0

I/O type: Pull-down, 5 V tolerant

This is the LSB bit of I²C slave address. The pin is internally pulled-down. Therefore, when the pin is open, SLVADR0 becomes 0.

Fix SLVADR0 before the hardware reset is negated.

Table 22: SLVADR0 truth table

SLVADR0	Description
0	Set LSB of the I2C slave address to 0.
1	Set LSB of the I2C slave address to 1.

SLVADR3

I/O type: Pull-up, 5 V tolerant

This is Bit 3 of I²C slave address. The pin is internally pulled-up. Therefore, when the pin is open, SLVADR3 becomes 1.

Fix SLVADR3 before the hardware reset is negated.

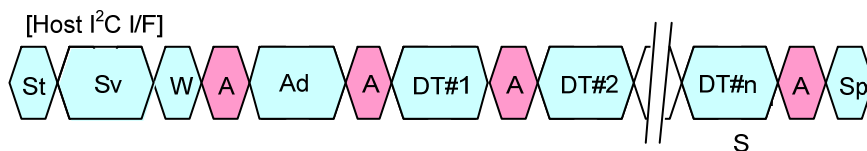
SLVADR3	Description
0	Set BIT 3 of the I2C slave address to 0.
1	Set BIT 3 of the I2C slave address to 1.

9.4.1. Host I²C Sequence

Writing/reading sequence from host CPU to this LSI is as follows.

It access to the same bank corresponds to continuous write and read.

I²C Write sequence



I²C Read sequence

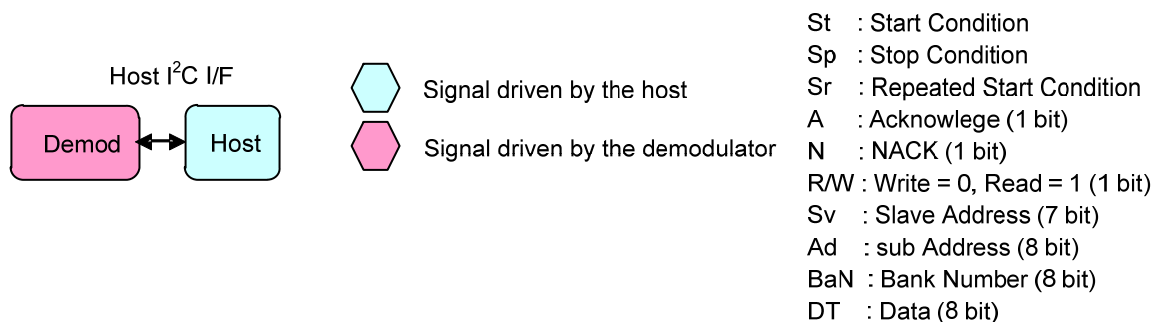
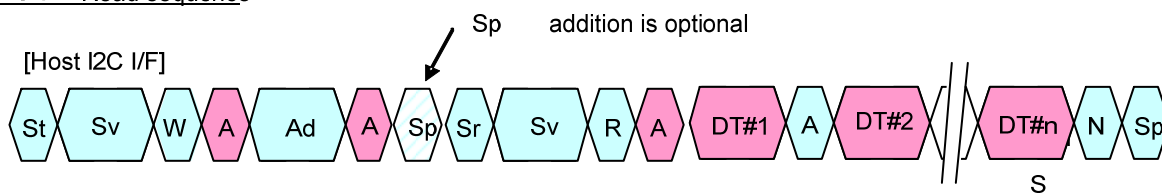


Fig.5. I²C Read/Write Sequence

9.4.2. I²C Gateway Sequence

Communication can be performed with tuners via the tuner I²C interface by writing and reading special address 09 h of this LSI from the host.

Please set the slave address of each demodulator corresponding to Tuner.

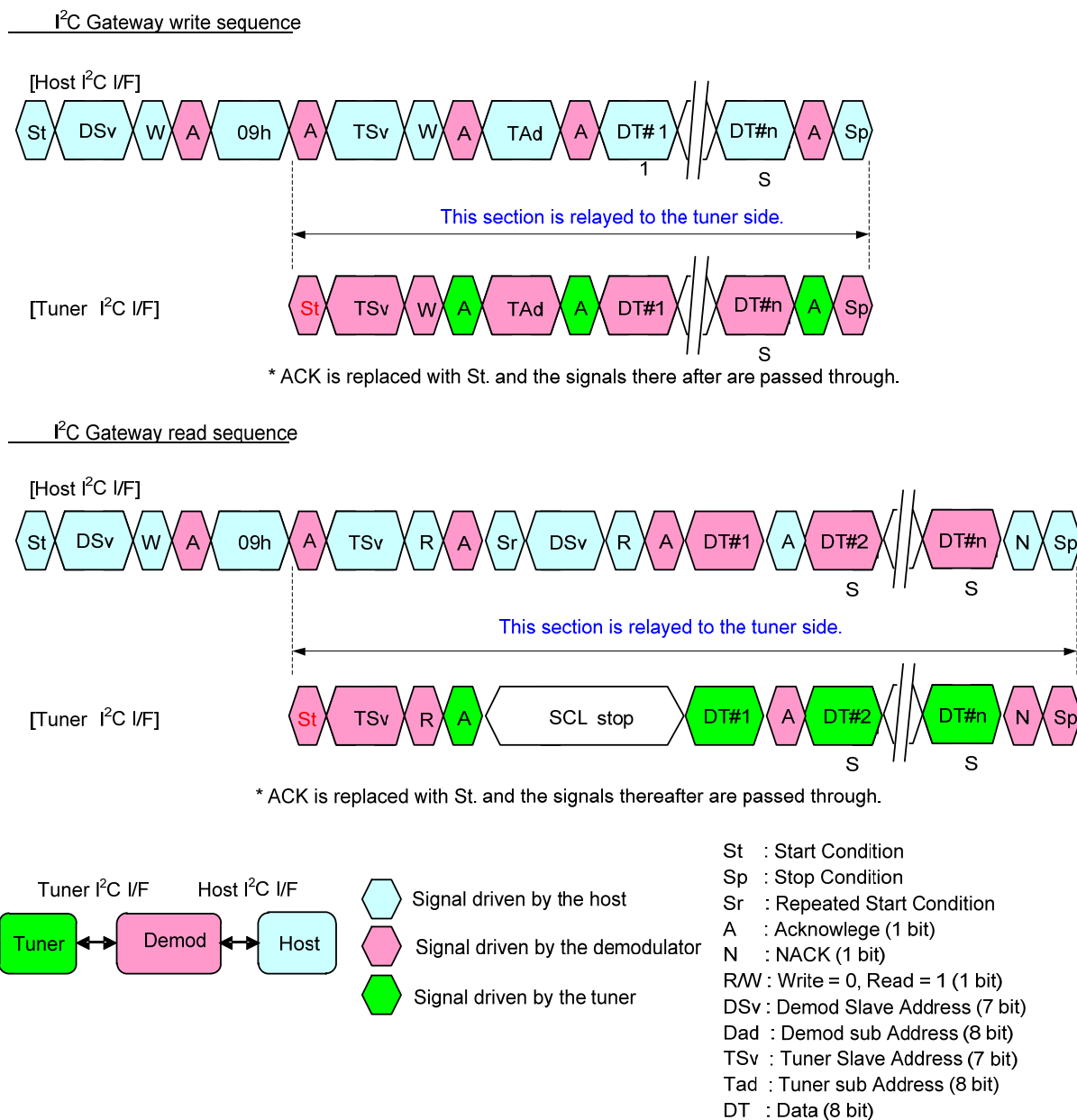


Fig.6. I²C Gateway Sequence

9.5. AGC Output Interface

Corresponding I/O names are: TIFAGC and GPIO1

TIFAGC and GPIO1 outputs the PWM signal that represents the IF input signal level.

TIFAGC is designed to share the TIFAGC with another demodulator e.g. analogue TV demodulator. The CXD2840ER allows the intermediate voltage input to TIFAGC (note: not GPIO1). The CXD2840ER can share the TIFAGC output by simply connecting the other AGC line. Set TIFAGC to high impedance using the register when the other demodulator is in operation.

TIFAGC

I/O type: n/a (CMOS output)

Initial condition: Hi-Z

This is the PWM output to control IF AGC gain.

CAUTION: This pin is not 5 V tolerant. Applying the voltage above DVDD+0.3 V to the port may cause damage to the CXD2840ER.

GPIO1 (PWM)

I/O type: Selectable Pull-up *1, 5 V tolerant

Initial condition: Hi-Z

*1 Pull-up enabled at default. The register can disable the pull-up

This is the PWM output to control RF AGC gain.

CAUTION: This pin is bidirectional I/O that does not allow intermediate voltage input. Applying the intermediate voltage may cause the penetration current to flow in the I/O and may cause damage to the CXD2840ER.

9.6. TS Output Interface

Corresponding I/O names are: TSCLK, TSVVALID, TSSYNC, and TSDATA[7:0]

These are the transport stream output pins.

The TS output can be selected to be either parallel output and serial output. The serial output can output the TSDATA from either TSDATA[7] or TSDATA[0]. The interface has the TS smoothing function that suppresses PCR jitter. Two output current modes are supported, these are selected by the control register. The CXD2840ER has internal pull-ups that can be enabled by the register setting. The internal pull-up is disabled in default.

Table 23: TS Output PCR Jitter Value

Symbol	Parallel output (default)	Serial output
TSSYNC	SYNC	SYNC
TSVALID	VALID	VALID
TSCLK	CLK	CLK
TSDATA0	DATA0	Low (*1)
TSDATA1	DATA1	Low (*1)
TSDATA2	DATA2	Low (*1)
TSDATA3	DATA3	Low (*1)
TSDATA4	DATA4	Low (*1)
TSDATA5	DATA5	Low (*1)
TSDATA6	DATA6	Low (*1)
TSDATA7	DATA7	DATA (*2)

*1. This IC can fix Hi-Z by the register setting.

*2. The serial TS data can be outputted from TSDATA0 by the register setting.

Table 24: TS Output PCR Jitter Value

Parameter	Target Value
PCR Jitter DTMB mode	$\pm 5 \mu\text{s}$
PCR Jitter DVB-C mode	$\pm 5 \mu\text{s}$

TSCLK, TSVVALID, TSSYNC, and TSDATA[7:0]

I/O type: Selectable Pull-up *1, Selectable Output Current *2

Initial condition: Hi-Z

*1 Pull-up disabled by default. The register can enable the pull-up.

*2 $I_{OLH} = 8 \text{ mA}$ by default. The register can set it to 10 mA.

9.7. General Purpose I/O

Corresponding I/O names are: GPIO0, GPIO1, and GPIO2

GPIO0, GPIO1, GPIO2

I/O type: Selectable Pull-up *1, 5 V tolerant

Initial condition: Hi-Z

*1 Pull-up enabled at default. The register can disable the pull-up

These are general purpose I/Os and the pins are directly connected to the internal I²C registers. GPIO1 and GPIO2 are multiplexed with the other function PWM and TSERR respectively.

9.8. Test pins

Corresponding I/O name is: TESTMODE

TESTMODE

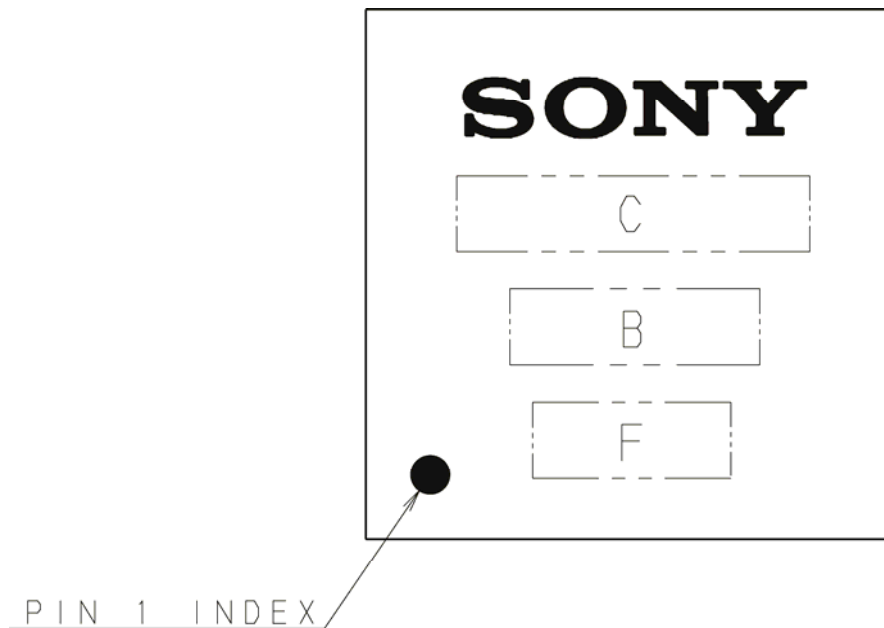
I/O type: Pull-down, 5 V tolerant

This pin is to set LSI testing mode. For normal operation, connect TESTMODE directly to GND.

Table 25: TESTMODE truth table

TESTMODE	Description
0	Set TESTMODE = 0 when in normal operation
1	TESTMODE = 1 is only for LSI testing purpose.

11. Marking



MARKING C: D2840ER

注1) C部は製品名 (Max 7文字) を配置する。

(7文字を超える場合は製品名省略標示規定に従う。)

2) B部はロット番号 (Max 5文字) を配置する。

3) F部は年コード (2文字)、週コード (2文字) を配置する。

< INSTRUCTIONS >

1) TYPE NO. (MAX 7 CHARACTERS) IN SECTION C.

(FOR MORE THAN 7 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

2) LOT NO. (MAX 5 CHARACTERS) IN SECTION B.

3) YEAR CODE (2 CHARACTERS)

WEEK CODE (2 CHARACTERS) IN SECTION F.

Note

Sony reserves the right to change products and specifications without prior notice.

This information does not convey any license by any implication or otherwise under any patents or other right.

Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.