
Absolute Maximum Ratings

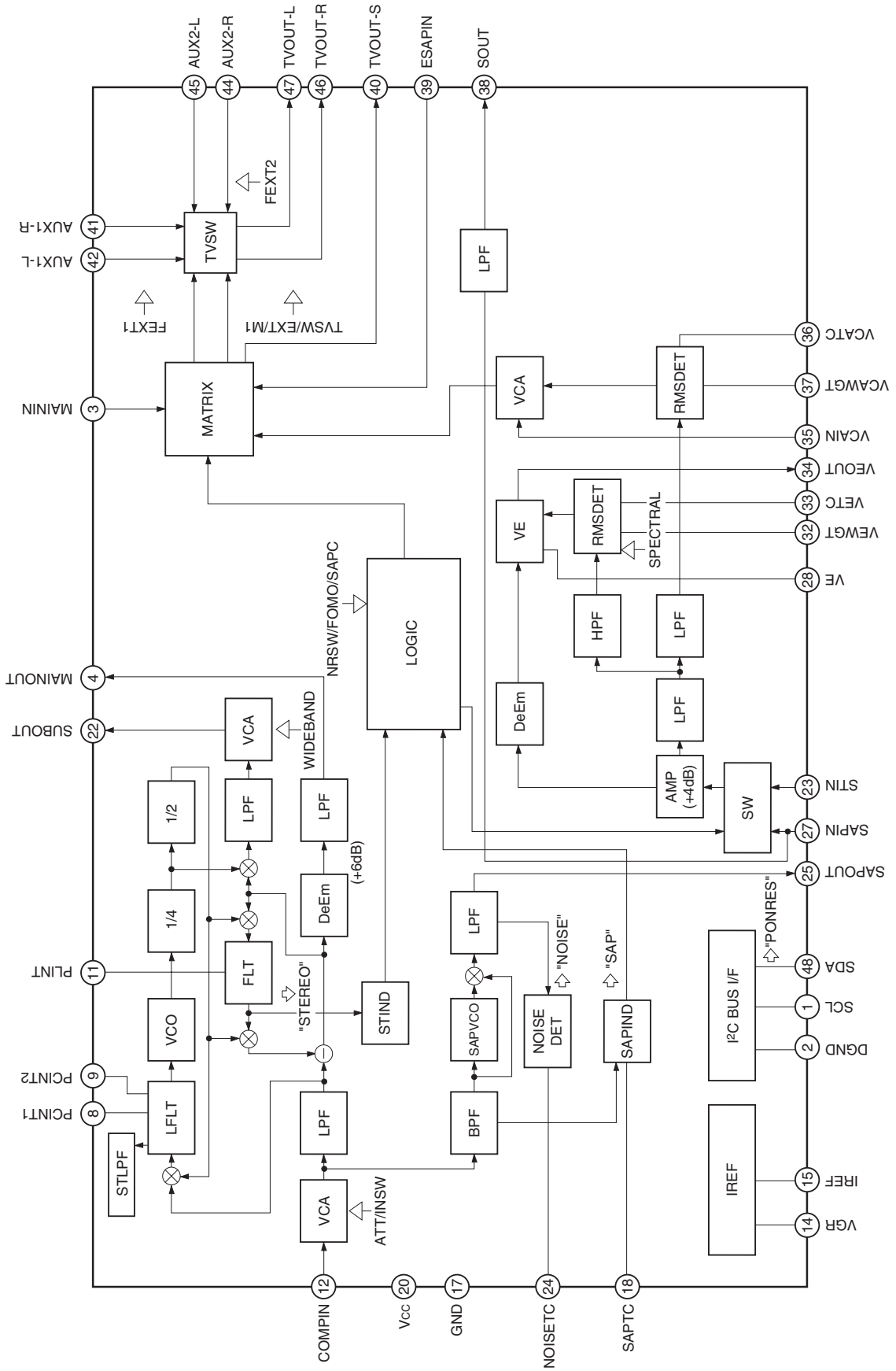
(Ta = 25°C)

◆ Supply voltage	Vcc	11	V
◆ Operating temperature	Topr	-20 to +75	°C
◆ Storage temperature	Tstg	-65 to +150	°C
◆ Allowable power dissipation	Pd	0.6	W

Range of Operating Supply Voltage

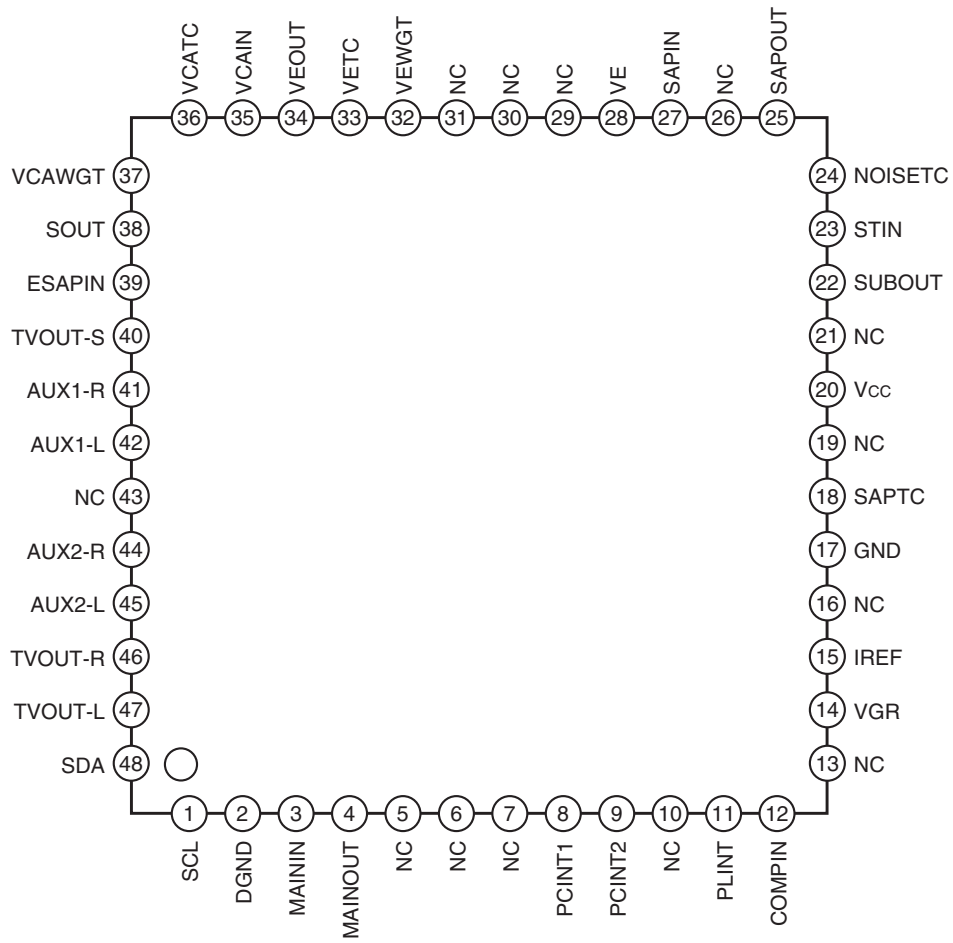
9 ± 0.5 V

Block Diagram



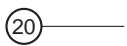
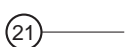
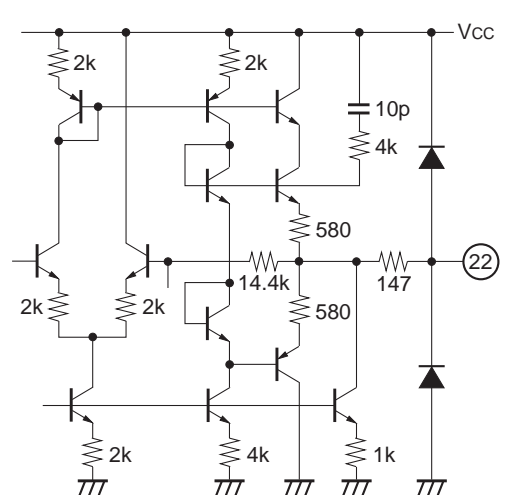
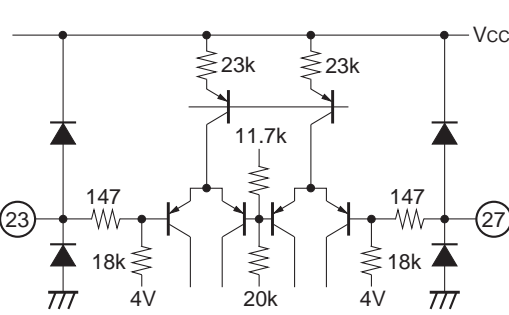
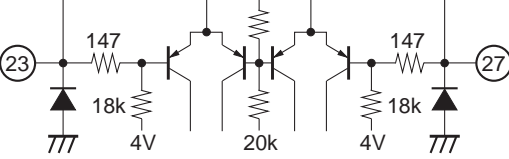
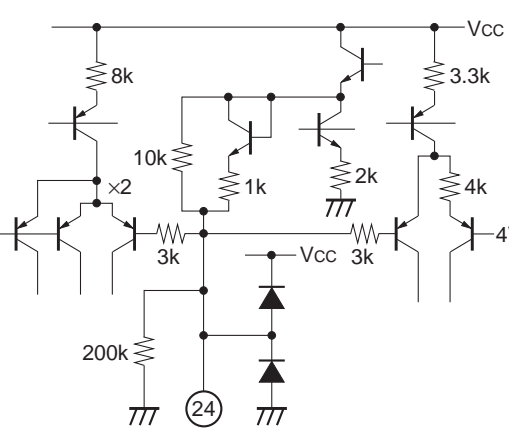
Pin Configuration

(Top View)



Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
8	PCINT1	4.0V		Stereo block PLL loop filter integrating pin.
9	PCINT2	4.0V		
10	NC	—		—
11	PLINT	5.1V		Pilot cancel circuit loop filter integrating pin. (Connect a 1 μ F capacitor between this pin and GND.)
12	COMPIN	4.0V		Audio multiplexing signal input pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
13	NC	—		—
14	VGR	1.3V		Band gap reference output pin. (Connect a 10 μ F capacitor between this pin and GND.)
15	IREF	1.3V		Set the filter and VCO reference current. The reference current is adjusted with the BUS DATA based on the current which flows to this pin. (Connect a 62k Ω (\pm 1%) resistor between this pin and GND.)
16	NC	—		—
17	GND	—		Analog block GND.
18	SAPTC	4.5V		Set the time constant for the SAP carrier detection circuit. (Connect a 4.7 μ F capacitor between this pin and GND.)
19	NC	—		—

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
20	Vcc	—		Supply voltage pin.
21	NC	—		—
22	SUBOUT	4.0V		(L – R) signal output pin.
23	STIN	4.0V		Input the (L – R) signal from SUBOUT (Pin 22).
27	SAPIN	4.0V		Input the (SAP) signal from SAPOUT (Pin 25).
24	NOISETC	3.0V		Set the time constant for the noise detection circuit. (Connect a 4.7μF capacitor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
25	SAPOUT	4.0V		SAP FM detector output pin.
26	NC	—		—
28	VE	4.0V		Variable de-emphasis integrating pin. (Connect a 2700pF capacitor and a 3.3kΩ resistor in series between this pin and GND.)
29	NC	—		—
30	NC	—		—
31	NC	—		—
32	VEWGT	4.0V		Weight the variable de-emphasis control effective value detection circuit. (Connect a 0.047μF capacitor and a 3kΩ resistor in series between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
33	VETC	1.7V		<p>Determine the restoration time constant of the variable de-emphasis control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 3.3µF capacitor between this pin and GND.)</p>
34	VEOUT	4.0V		<p>Variable de-emphasis output pin. (Connect a 4.7µF non-polar capacitor between Pins 34 and 35.)</p>
35	VCAIN	4.0V		<p>VCA input pin. Input the variable de-emphasis output signal from Pin 34 via a coupling capacitor.</p>
36	VCATC	1.7V		<p>Determine the restoration time constant of the VCA control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 10µF capacitor between this pin and GND.)</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
37	VCAWGT	4.0V		<p>Weight the VCA control effective value detection circuit. (Connect a 1 μF capacitor and a 3.9kΩ resistor in series between this pin and GND.)</p>
38	SOUT	4.0V		<p>Additional SAP output pin.</p>
39	ESAPIN	4.0V		<p>Input the signal from SOUT (Pin 38).</p>
41	AUX1-R	4.0V		<p>Right channel external input 1 pin.</p>
42	AUX1-L	4.0V		<p>Left channel external input 1 pin.</p>
44	AUX2-R	4.0V		<p>Right channel external input 2 pin.</p>
45	AUX2-L	4.0V		<p>Left channel external input 2 pin.</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
40	TVOUT-S	4.0V		Optional output pin. From this pin monaural or additional SAP is output.
46	TVOUT-R	4.0V		TVOUT right channel output pin.
47	TVOUT-L	4.0V		TVOUT left channel output pin.
43	NC	—		—
48	SDA	—		Serial data I/O pin. $V_{IH} > 3.0V$ $V_{IL} < 1.5V$

Electrical Characteristics

COMPIN input level (100% modulation level)

	INSW = 0	INSW = 1
Main (L + R) (Pre-emphasis: OFF)	= 245mVrms	= 100mVrms
SUB (L - R) (dbx-TV: OFF)	= 490mVrms	= 200mVrms
Pilot	= 49mVrms	= 20mVrms
SAP carrier	= 147mVrms	= 60mVrms

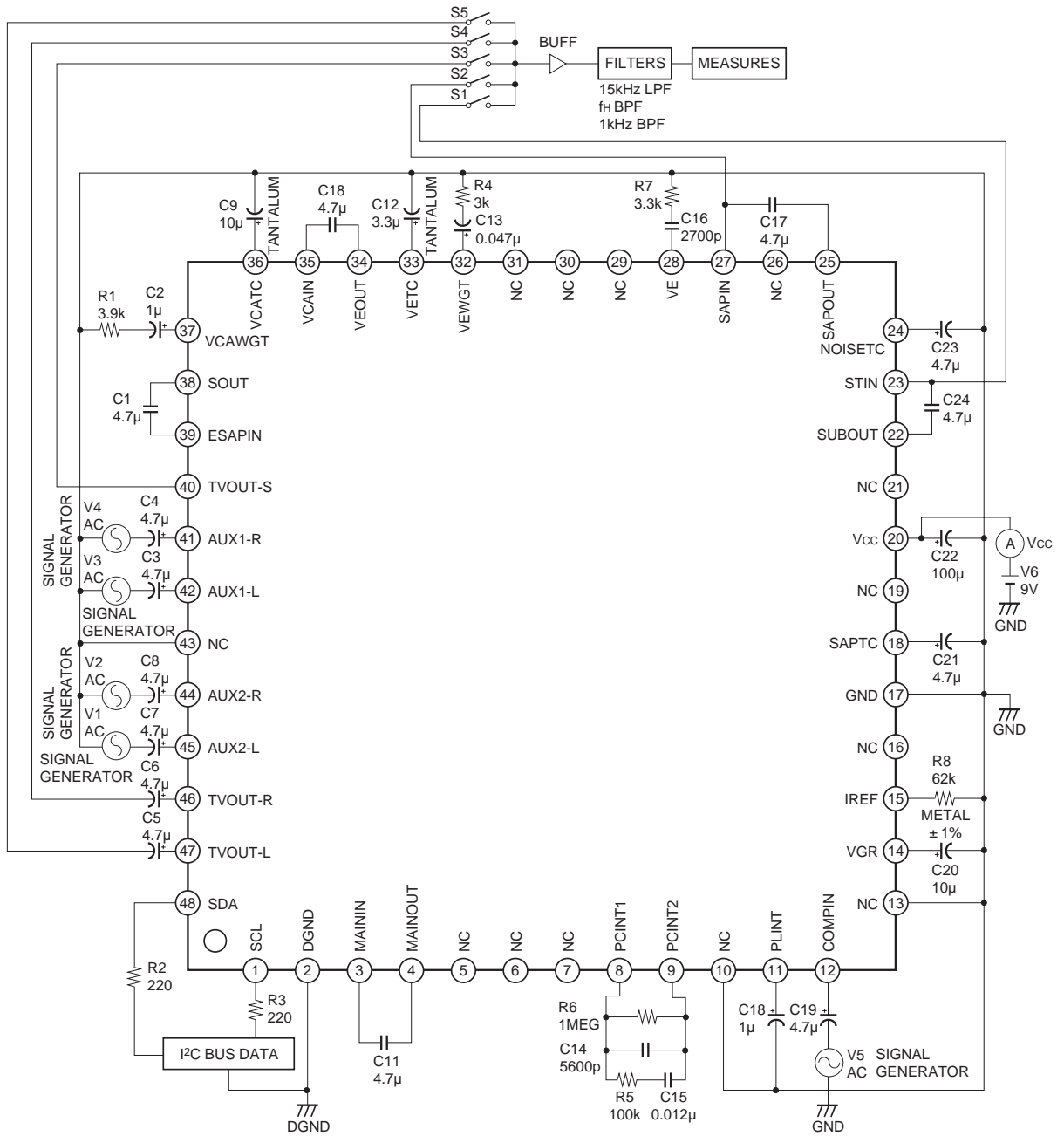
f_H = 15.734kHz

(T_a = 25°C, V_{cc} = 9V)

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
1	Current consumption	I _{cc}		—	No signal				22	32	42	mA
2	Main output level	V _{main}	MONO	12	Mono 1kHz, 100% mod. Pre-em. ON			46/47	440	490	540	mVrms
3	Main de-emphasis frequency characteristic	FC _{deem}	MONO	12	Mono 5kHz, 30% mod. Pre-em. ON	20 log ('5k'/'1k')		46/47	-1.2	0	1.0	dB
4	Main LPF frequency characteristic	FC _{main}	MONO	12	Mono 12kHz, 30% mod. Pre-em. ON	20 log ('12k'/'1k')		46/47	-3.0	-1.0	1.0	dB
5	Main distortion	THD _m	MONO	12	Mono 1kHz, 100% mod. Pre-em. ON		15kLPF	46/47	—	0.1	0.5	%
6	Main overload distortion	THD _{mmax}	MONO	12	Mono 1kHz, 200% mod. Pre-em. OFF		15kLPF	46/47	—	0.15	0.5	%
7	Main S/N	SN _{main}	MONO	12	Mono 1kHz, Pre-em. ON	20 log ('100%'/'0%')	15kLPF	46/47	61	69	—	dB
8	Sub output level	V _{sub}	ST	12	SUB (L - R) 1kHz, 100% mod., NR OFF			22	150	190	230	mVrms
9	Sub LPF frequency characteristic	FC _{sub}	ST	12	SUB (L - R) 12kHz, 30% mod., NR OFF	20 log ('12k'/'1k')		22	-3.0	-0.5	1.0	dB
10	Sub distortion	THD _{sub}	ST	12	SUB (L - R) 1kHz, 100% mod., NR OFF		15kLPF	22	—	0.1	1.0	%
11	Sub overload distortion	THD _{smax}	ST	12	SUB (L - R) 1kHz, 200% mod., NR OFF		15kLPF	22	—	0.2	2.0	%
12	Sub S/N	SN _{sub}	ST	12	SUB (L - R) 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	22	56	64	—	dB
13	ST → SAP crosstalk	CT _{st}	SAP	12	SUB (L - R) 1kHz, 100% mod., NR ON, SAP carrier (5f _H)	20 log ('NRSW = 0'/'NRSW = 1')	1kBPF	47	60	70	—	dB
14	Sub pilot leak	PC _{sub}	ST	12	PILOT (f _H) 0dB	0dB = 49mVrms	f _H BPF	22	—	-42	-30	dB
15	Stereo ON level	TH _{st}	ST	12	Change PILOT (f _H) level	0dB = 49mVrms	BUS RETURN	-9.0	-6.0	-3.0	dB	
16	Stereo ON/OFF hysteresis	HY _{st}				20 log ('on level'/'off level')		2.0	6.0	10.0	dB	
17	SAP output level	V _{sap}	SAP	12	SAP 1kHz, 100% mod. NR OFF			25	150	190	230	mVrms
18	SAP LPF frequency characteristic	FC _{sap}	SAP	12	SAP 10kHz, 30% mod. NR OFF	20 log ('10k'/'1k')		25	-3.0	0	2.5	dB
19	SAP distortion	THD _{sap}	SAP	12	SAP 1kHz, 100% mod. NR OFF		15kLPF	25	—	2.5	6.0	%
20	SAP S/N	SN _{sap}	SAP	12	SAP 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	25	46	55	—	dB

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
21	SAP → ST cross talk	CTsap	ST	12	SAP 1kHz, 100% mod. NR ON, PILOT (fH)	20 log (‘NRSW = 1’/ ‘NRSW = 0’)	1kBPF	47	60	70	—	dB
22	SAP ON level	THsap	SAP	12	Change SAP carrier (5fH) level	0dB = 147mVrms		BUS RETURN	-12.0	-9.0	-6.5	dB
23	SAP ON/OFF hysteresis	HYsap				20 log (‘on level’/ ‘off level’)			2.0	4.0	6.0	dB
24	ST separation 1 L → R	STLsep1	ST	12	ST-L 300Hz, 30% mod. NR ON		15kLPF	46/47	23	35	—	dB
25	ST separation 1 R → L	STRsep1	ST	12	ST-R 300Hz, 30% mod. NR ON		15kLPF	46/47	23	35	—	dB
26	ST separation 2 L → R	STLsep2	ST	12	ST-L 3kHz, 30% mod. NR ON		15kLPF	46/47	23	35	—	dB
27	ST separation 2 R → L	STRsep2	ST	12	ST-R 3kHz, 30% mod. NR ON		15kLPF	46/47	23	35	—	dB
28	TVOUT output level	Vtv	EXT	41/42 44/45	Sine wave 1kHz, 490mVrms	0dB = 490mVrms		46/47	-0.5	0	0.5	dB
29	TVOUT cross talk	CTtv1	INT	41/42 44/45	Sine wave 1kHz, 490mVrms	0dB = 490mVrms EXT → INT	1kBPF	46/47	—	-75	-60	dB
30		CTtv2	EXT	12	MONO 1kHz, 100% mod. Pre-em. ON	0dB = 490mVrms INT → EXT	1kBPF	46/47	—	-90	-80	dB
31	TVOUT muted amount	MUtv1	INT	12	MONO 1kHz, 100% mod. Pre-em. ON	20 log (M1 = “0”/ M1 = “1”)	1kBPF	46/47	—	-85	-70	dB
32		MUtv2	EXT	41/42 44/45	Sine wave 1kHz, 490mVrms	20 log (M1 = “0”/ M1 = “1”)			—	-90	-75	dB
33	TVOUT DC offset	OSTv	INT EXT	—	No signal	Mute (M1 = 0)/ DC difference when there is no signal		46/47	-25	0	25	mV
34	TVOUT distortion	THDtv	EXT	41/42 44/45	Sine wave 1kHz, 490mVrms		15kLPF	46/47	—	0.01	0.5	%
35	TVOUT S/N	SNtv	EXT	41/42 44/45	Sine wave 1kHz, 490mVrms	20 log (‘490mVrms’/ ‘No signal’)	15kLPF	46/47	75	88	—	dB
36	TVOUT overload distortion	THDtvmax	EXT	41/42 44/45	Sine wave 1kHz, 2Vrms		15kLPF	46/47	—	0.1	1.0	%

Electrical Characteristics Measurement Circuit



**Adjustment Method (Input signal level is the case when standard input signal is 245mVrms)**

1. ATT adjustment
 - (1) TEST BIT is set to "TEST1 = 0" and "TEST-DA = 0".
 - (2) Input a 100Hz, 245mVrms sine wave signal to COMPIN and monitor the TVOUT-L output level. Then, adjust the "ATT" data for ATT adjustment so that the TVOUT-L output goes to the standard value (490mVrms).
 - (3) Adjustment range: $\pm 30\%$
Adjustment bits: 4 bits
2. Separation adjustment
 - (1) TEST BIT is set to "TEST1 = 0" and "TEST-DA = 0".
 - (2) Set the unit to stereo mode and input the left channel only signal (modulation factor 30%, frequency 300Hz NR-ON) to COMPIN. At this time, adjust the "WIDEBAND" adjustment data to reduce TVOUT-R output to the minimum.
 - (3) Next, set the frequency only of the input signal to 3kHz and adjust the "SPECTRAL" adjustment data to reduce TVOUT-R output to the minimum.
 - (4) The adjustments in 2 and 3 above are performed to optimize the separation.
 - (5) ♦ WIDEBAND
Adjustment range: $\pm 30\%$
Adjustment bits: 6 bits
♦ SPECTRAL
Adjustment range: $\pm 15\%$
Adjustment bits: 6 bits

Note) Adjust this through Tuner and IF when this IC is mounted on the set.

Description of Operation

The US audio multiplexing system possesses the base band spectrum shown in Fig. 1.

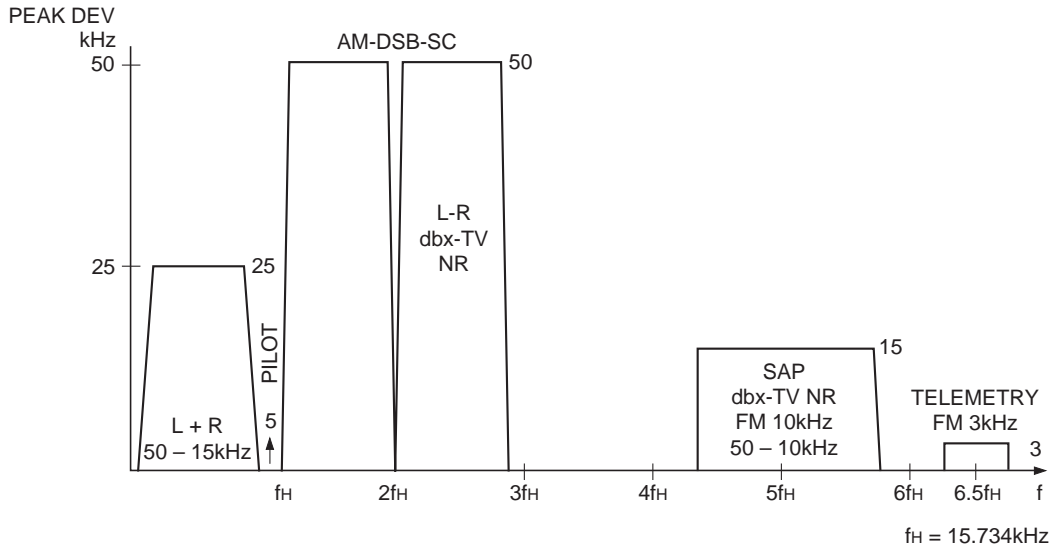


Fig. 1. Base band spectrum

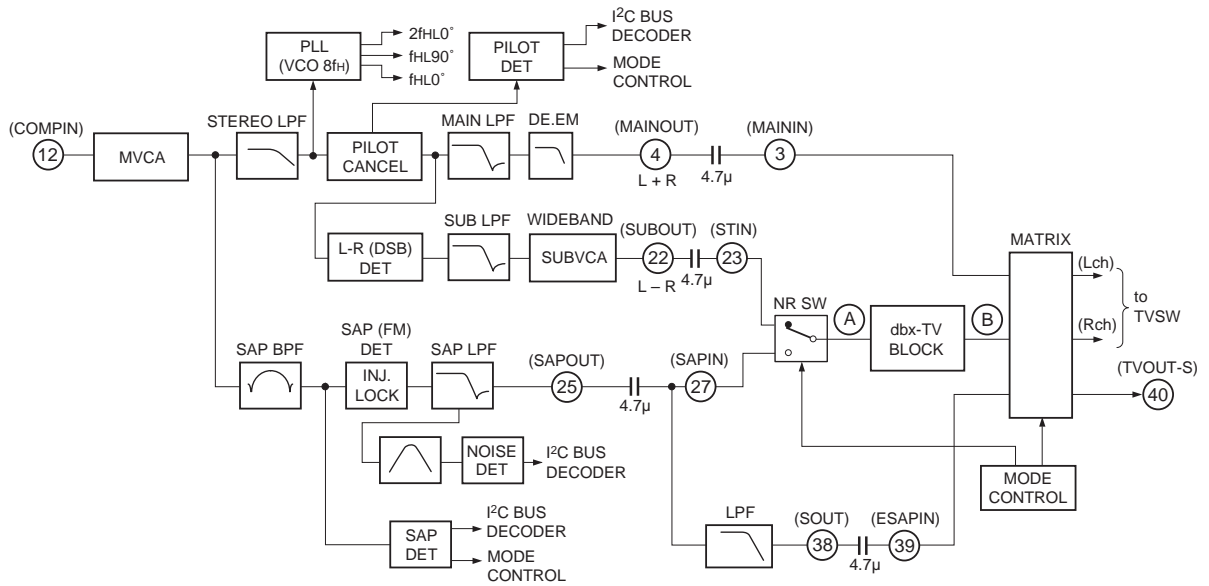


Fig. 2. Overall block diagram (See Fig. 3 for the dbx-TV block)

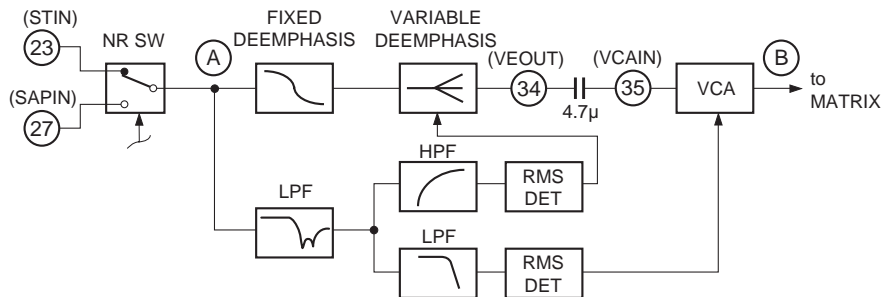


Fig 3. dbx-TV block

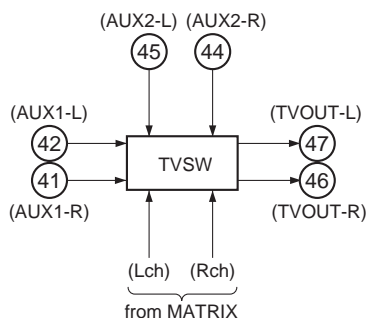


Fig. 4. Switch block

1. L + R (MAIN)

After the audio multiplexing signal input from COMPIN (Pin 12) passes through MVCA, the SAP signal and telemetry signal are suppressed by STEREO LPF. Next, the pilot signals are canceled. Finally, the L – R signal and SAP signal are removed by MAIN LPF, and frequency characteristics are flattened (de-emphasized) and input to the matrix.

2. L – R (SUB)

The L – R signal follows the same course as L + R before the pilot signal is canceled. L – R has no carrier signal, as it is a suppressed-carrier double-sideband amplitude modulated signal (DSB-AM modulated). For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for the demodulation of the L – R signal. In the last stage, the residual high frequency components are removed by SUB LPF and the L – R signal is input to the dbx-TV block via the NRSW circuit after passing through SUBVCA.

3. SAP

SAP is an FM signal using 5fH as a carrier as shown in the Fig. 1. First, the SAP signal only is extracted using SAP BPF. Then, this is subjected to FM detection. Finally, residual high frequency components are removed and frequency characteristics flattened using SAP LPF, and the SAP signal is input to the dbx-TV block via the NRSW circuit. When there is no SAP signal, the Pin 25 output is soft muted.

4. Mode discrimination

Stereo discrimination is performed by detecting the pilot signal amplitude. SAP discrimination is performed by detecting the 5fH carrier amplitude. NOISE discrimination is performed by detecting the noise near 25kHz after FM detection of SAP signal.

5. dbx-TV block

Either the L – R signal or SAP signal input respectively from ST IN (Pin 23) or SAP IN (Pin 27) is selected by the mode control and input to the dbx-TV block.

The input signal then passes through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The signal output from the variable de-emphasis circuit passes through an external capacitor and is applied to VCA (voltage control amplifier). Finally, the VCA output is converted from a current to a voltage using an operational amplifier and then input to the matrix.

The variable de-emphasis circuit transmittance and VCA gain are respectively controlled by each of effective value detection circuits. Each of the effective value detection circuits passes the input signal through a predetermined filter for weighting before the effective value of the weighted signal is detected to provide the control signal.

6. Matrix, TVSW

The signals (L + R, L – R, SAP) input to “MATRIX” become the outputs for the ST-L, ST-R, MONO and SAP signals according to the mode control and whether there is ST / SAP discrimination.

“TVSW” switches the “MATRIX” output signal, external input signal (input to AUX1-L, R (Pins 42 and 41)), external input signal (input to AUX2-L, R (Pins 45 and 44)) and external forced MONO.

7. Others

“MVCA” is a VCA which adjusts the input signal level to the standard level of this IC.

“Bias” supplies the reference voltage and reference current to the other blocks. The current flowing to the resistor connecting IREF (Pin 15) with GND become the reference current.



Register Specifications

Slave address

SLAVE RECEIVER	SLAVE TRANSMITTER
84H (1000 0100)	85H (1000 0101)

Register table

SUB ADDRESS		DATA							
MSB	LSB	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
****0000		*		TEST-DA	TEST1	ATT (4)			
****0001		*		SPECTRAL (6)					
****0010		*		WIDEBAND (6)					
****0011		*		TVSW	EXT	NRSW	FOMO	SAPC	M1
****0100		*		INSW	SMD	ATTSW	FST	FEXT1	FEXT2

*: Don't care

Status registers

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	—	—	—	—

Description of Registers

Control registers

Register	Number of bits	Classification*1	Standard setting	Contents
ATT	4	A	9	Input level adjustment
SPECTRAL	6	A	1F	Adjustment of stereo separation (3kHz)
WIDEBAND	6	A	1F	Adjustment of stereo separation (300Hz)
TEST-DA	1	T	0	Turn to DAC test mode and VCO adjustment mode by means of TEST-DA = 1.
TEST1	1	T	0	Turn to test mode by means of TEST = 1. (Adjustment of FILTER)
FST	1	T	0	Turn to forced stereo by means of FST = 1.
NRSW	1	U	—	Selection of the output signal (Stereo mode, SAP mode)
FOMO	1	U	—	Turn to forced MONO by means of FOMO = 1. (Left channel only is MONO during SAP output.)
TVSW	1	U	0	Selection of TV mode or external input mode for TVOUT output
FEXT1	1	U	0	External input 1 forced MONO (1: forced MONO ON)
FEXT2	1	U	0	External input 2 forced MONO (1: forced MONO ON)
EXT	1	U	0	Selection of external input 1 mode or external input 2 mode for TVOUT output. (TVSW = 1)
M1	1	U	1	Selection of TVOUT mute ON/OFF (0: mute ON, 1: mute OFF)
SMD	1	U	0	Selection of L + R or additional SAP
ATTSW	1	S	—	Turn the input stage MVCA off when ATTSW = 1.
INSW	1	S	—	Selection of standard input level
SAPC	1	S	—	Selection of SAP mode or L + R mode according to the presence of SAP broadcasting

*1 Classification U: User control
 A: Adjustment
 S: Proper to set
 T: Test

Status registers

Register	Number of bits	Contents
PONRES	1	POWER ON RESET detection; 1: RESET
STEREO	1	Stereo discrimination of the COMPIN input signal; 1: Stereo
SAP	1	SAP discrimination of the COMPIN input signal; 1: SAP
NOISE	1	Noise level discrimination of the SAP signal; 1: Noise

Note) When the IC is powered on, all registers are set to "0".

Description of Control Registers

- ATT (4): Adjust the signal level input to COMPIN (Pin 12) to the standard input level.
Variable range of the input signal: standard input level -5.0dB to +3.0dB
0 = Level min.
F = Level max.
- SPECTRAL (6): Perform high frequency (fs = 3kHz) separation adjustment.
0 = Level max.
3F = Level min.
- WIDEBAND (6): Perform low frequency (fs = 300Hz) separation adjustment.
0 = Level min.
3F = Level max.
- TEST-DA (1): Set DAC output test mode.
0 = Normal mode
1 = DAC output test mode
In addition, the following output are present at Pin 47.
TVOUT-L (Pin 47): DA control DC level
- TEST1 (1): Monitor SAP BPF and NR BPF output.
0 = Normal mode
1 = SAP BPF and NR BPF output
In addition, the following outputs are present at Pins 47 and 46.
TVOUT-L (Pin 47): SAP BPF OUT
TVOUT-R (Pin 46): NR BPF OUT
- FST (1): Select forced STEREO mode
0 = Normal mode
1 = Forced stereo mode
- NRSW (1): Select stereo mode or SAP mode
0 = Stereo mode
1 = SAP mode
- FOMO (1): Select forced MONO mode
0 = Normal mode
1 = Forced MONO mode
- FEXT1 (1): Turn external input [1] to forced MONO
0 = Normal mode
1 = External input [1] is forced MONO
Input the same signal to both AUX1-L and AUX1-R.
- FEXT2 (1): Turn external input [2] to forced MONO
0 = Normal mode
1 = External input [2] is forced MONO
Input the same signal to both AUX2-L and AUX2-R.
- TVSW (1): Select TV mode or external input mode for TVOUT output.
0 = TV mode
1 = External input mode
- EXT (1): Select external input [1] mode or external input [2] mode for TVOUT output. (TVSW = 1)
0 = External input [1] mode
1 = External input [2] mode
- M1 (1): Mute the TVOUT-L and TVOUT-R output.
0 = Mute ON
1 = Mute OFF

SMD (1):	Select L + R or additional SAP signal 0 = L + R output is selected 1 = Additional SAP output is selected
ATTSW (1):	Select BYPASS SW of MVCA 0 = Normal mode 1 = MVCA is passed
INSW (1):	Select standard input level of COMPIN (Pin 12) 0 = 245mVrms 1 = 100mVrms
SAPC (1):	Select the SAP signal output mode When there is no SAP signal, the conditions for selecting SAP output are selected by SAPC. 0 = L + R output is selected 1 = SAP output is selected

Description of status registers SAP/NOISE

The microcomputer reads both SAP and NOISE status and judges SAP discrimination.

SAP = 0, NOISE = 0: NO SAP
SAP = 1, NOISE = 0: SAP
SAP = 0, NOISE = 1: NO SAP
SAP = 1, NOISE = 1: NO SAP

Description of Mode Control

Priority ranking: M1 > TVSW/EXT > (NRSW & FOMO & SAPC)

Mode control	SAPC = 0	SAPC = 1
NRSW	<p>“Select dbx input and TV decoder output”</p> <p>Conditions: FOMO = 0</p> <p>NRSW = 0 (MONO or ST output)</p> <ul style="list-style-type: none"> ◆ During ST input: left channel: L, right channel: R ◆ During other input: left channel: L + R, right channel: L + R <p>NRSW = 1 (SAP output)</p> <ul style="list-style-type: none"> ◆ When there is “SAP” during SAP discrimination – left channel: SAP, right channel: SAP ◆ When there is “No SAP”, output is the same as when NRSW = 0. 	<p>“Select dbx input and TV decoder output”</p> <p>Conditions: FOMO = 0</p> <p>NRSW = 0 (MONO or ST output)</p> <p>As on the left</p> <p>NRSW = 1 (SAP output)</p> <ul style="list-style-type: none"> ◆ Regardless of the presence of SAP discrimination, dbx input: “SAP” left channel: SAP, right channel: SAP <p>However, when there is no SAP, SAPOUT output is soft muted (–7dB).</p>
FOMO	<p>“Forced MONO”</p>	
	<p>FOMO = 1</p> <ul style="list-style-type: none"> ◆ During SAP output: left channel: L + R, right channel: SAP ◆ During ST or MONO output: left channel: L + R, right channel: L + R 	
SAPC	<p>Change the selection conditions for “MONO or ST output” and “SAP output”.</p> <p>SAPC = 0: Switch to SAP output when there is SAP discrimination. Do not switch to SAP output when there is no SAP discrimination.</p> <p>SAPC = 1: Switch to SAP output regardless of whether there is SAP discrimination.</p>	
M1	<p>“MUTE”</p>	
	<p>M1 = 0: TVOUT-L, R, S output is muted.</p>	
TVSW/EXT	<p>“TV mode/external input mode selection”</p>	
	<p>TVSW = 0: Set TVOUT-L, R output to TV mode.</p> <p>TVSW = 1: Set TVOUT-L, R output to external input mode.</p> <p>EXT = 0: Set TVOUT-L, R output to external input [1] mode. (TVSW = 1)</p> <p>EXT = 1: Set TVOUT-L, R output to external input [2] mode. (TVSW = 1)</p>	

Decoder Output and Mode Control Table 1 (SAPC = 1)

Input signal mode	Mode detection			Mode control			dbx input	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC		Lch	Rch
MONO*1	0	0	0	0	*	1	MUTE	L + R	L + R
	0	0	0	1	0	1	SAP	SAP	SAP
	0	0	0	1	1	1	SAP	L + R	SAP
	0	*	1	0	*	1	MUTE	L + R	L + R
	0	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	*	1	1	1	1	(SAP)	L + R	(SAP)
STEREO*1	1	0	*	0	0	1	L - R	L	R
	1	0	*	0	1	1	MUTE	L + R	L + R
	1	1	1	0	0	1	L - R	L	R
	1	1	1	0	1	1	MUTE	L + R	L + R
	1	0	0	1	0	1	SAP	SAP	SAP
	1	0	0	1	1	1	SAP	L + R	SAP
	1	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	*	1	1	1	1	(SAP)	L + R	(SAP)
MONO & SAP	0	1	*	0	0	1	MUTE	L + R	L + R
	0	1	*	0	1	1	MUTE	L + R	L + R
	0	1	0	1	0	1	SAP	SAP	SAP
	0	1	0	1	1	1	SAP	L + R	SAP
	0	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	1	(SAP)	L + R	(SAP)
STEREO & SAP	1	1	*	0	0	1	L - R	L	R
	1	1	*	0	1	1	MUTE	L + R	L + R
	1	1	0	1	0	1	SAP	SAP	SAP
	1	1	0	1	1	1	SAP	L + R	SAP
	1	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	1	(SAP)	L + R	(SAP)

Note) (SAP): The SAPOUT output signal is soft muted (approximately -7dB).
 The signal is soft muted when NOISE = 1.
 *: Don't care

*1 SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
 Then microcomputer reads "NOISE" status from IC and decides whether SAP is outputted.
 "NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Decoder Output and Mode Control Table 2 (SAPC = 0)

Input signal mode	Mode detection			Mode control			dbx input	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC		Lch	Rch
MONO* ¹	0	0	*	*	*	0	MUTE	L + R	L + R
	0	1	1	0	0	0	MUTE	L + R	L + R
	0	1	1	0	1	0	MUTE	L + R	L + R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L + R	(SAP)
STEREO* ¹	1	0	*	0	0	0	L - R	L	R
	1	0	*	0	1	0	MUTE	L + R	L + R
	1	0	*	1	0	0	L - R	L	R
	1	0	*	1	1	0	MUTE	L + R	L + R
	1	1	1	0	0	0	L - R	L	R
	1	1	1	0	1	0	MUTE	L + R	L + R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
MONO & SAP	0	1	0	0	0	0	MUTE	L + R	L + R
	0	1	0	0	1	0	MUTE	L + R	L + R
	0	1	0	1	0	0	SAP	SAP	SAP
	0	1	0	1	1	0	SAP	L + R	SAP
	0	1	1	0	0	0	MUTE	L + R	L + R
	0	1	1	0	1	0	MUTE	L + R	L + R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L + R	(SAP)
STEREO & SAP	1	1	0	0	0	0	L - R	L	R
	1	1	0	0	1	0	MUTE	L + R	L + R
	1	1	0	1	0	0	SAP	SAP	SAP
	1	1	0	1	1	0	SAP	L + R	SAP
	1	1	1	0	0	0	L - R	L	R
	1	1	1	0	1	0	MUTE	L + R	L + R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L + R	(SAP)

Note) (SAP): The SAPOUT output signal is soft muted (approximately -7dB).

The signal is soft muted when NOISE = 1.

*: Don't care

*¹ SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.

Then microcomputer reads "NOISE" status from IC and decides whether SAP is outputted.

"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Mode Control Table 3

	M1	TVSW	EXT	FEXT1	FEXT2	TVOUT-L	TVOUT-R
1	0	—	—	—	—	MUTE	MUTE
2	1	0	—	—	—	TV (L)	TV (R)
3	1	1	0	0	—	AUX1-L	AUX1-R
4	1	1	0	1	—	AUX1-L	AUX1-L
5	1	1	1	—	0	AUX2-L	AUX2-R
6	1	1	1	—	1	AUX2-L	AUX2-L

TV (L) / TV (R) are selected in MATRIX

TV (L): MONO, ST-L, SAP (SAPBPF out, D/A out)

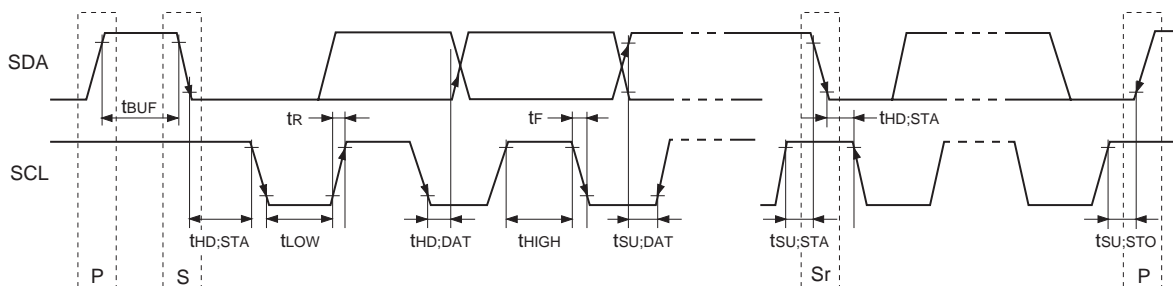
TV (R): MONO, ST-R, SAP (NRBPF out, STVCO freerun (4fH))

I²C BUS Block Items (SDA, SCL)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V _{IH}	3.0	—	5.0	V
2	Low level input voltage	V _{IL}	0	—	1.5	
3	High level input current	I _{IH}	—	—	10	μA
4	Low level input current	I _{IL}	—	—	10	
5	Low level output voltage SDA (Pin 48) during 3mA inflow	V _{OL}	0	—	0.4	V
6	Maximum inflow current	I _{OL}	3	—	—	mA
7	Input capacitance	C _i	—	—	10	pF
8	Maximum clock frequency	f _{SCL}	0	—	100	kHz
9	Minimum waiting time for data change	t _{BUF}	4.7	—	—	μs
10	Minimum waiting time for start of data transfer	t _{HD;STA}	4.0	—	—	
11	Low level clock pulse width	t _{LOW}	4.7	—	—	
12	High level clock pulse width	t _{HIGH}	4.0	—	—	
13	Minimum waiting time for start preparation	t _{SU;STA}	4.7	—	—	
14	Minimum data hold time	t _{HD;DAT}	0	—	—	
15	Minimum data preparation time	t _{SU;DAT}	250	—	—	ns
16	Rise time	t _R	—	—	1	μs
17	Fall time	t _F	—	—	300	ns
18	Minimum waiting time for stop preparation	t _{SU;STO}	4.7	—	—	μs

I²C BUS load conditions: Pull-up resistor 4kΩ (Connect to +5V)
 Load capacity 200pF (Connect to GND)

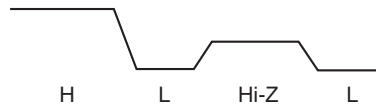
I²C BUS Control Signal



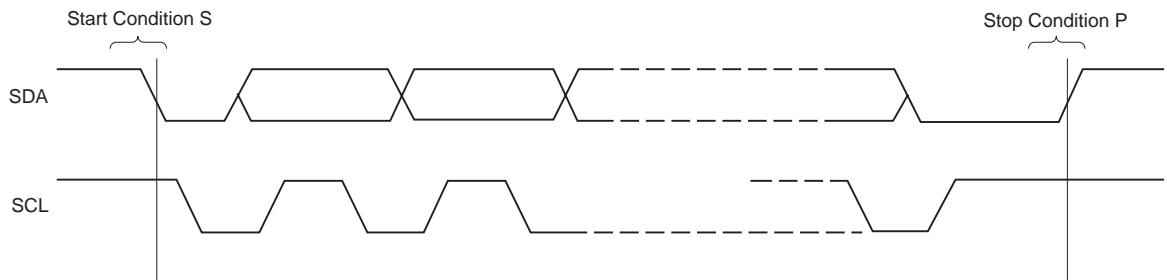
I²C BUS Signal

There are two I²C signals, SDA (Serial DATA) and SCL (Serial CLOCK) signals. SDA is a bidirectional signal.

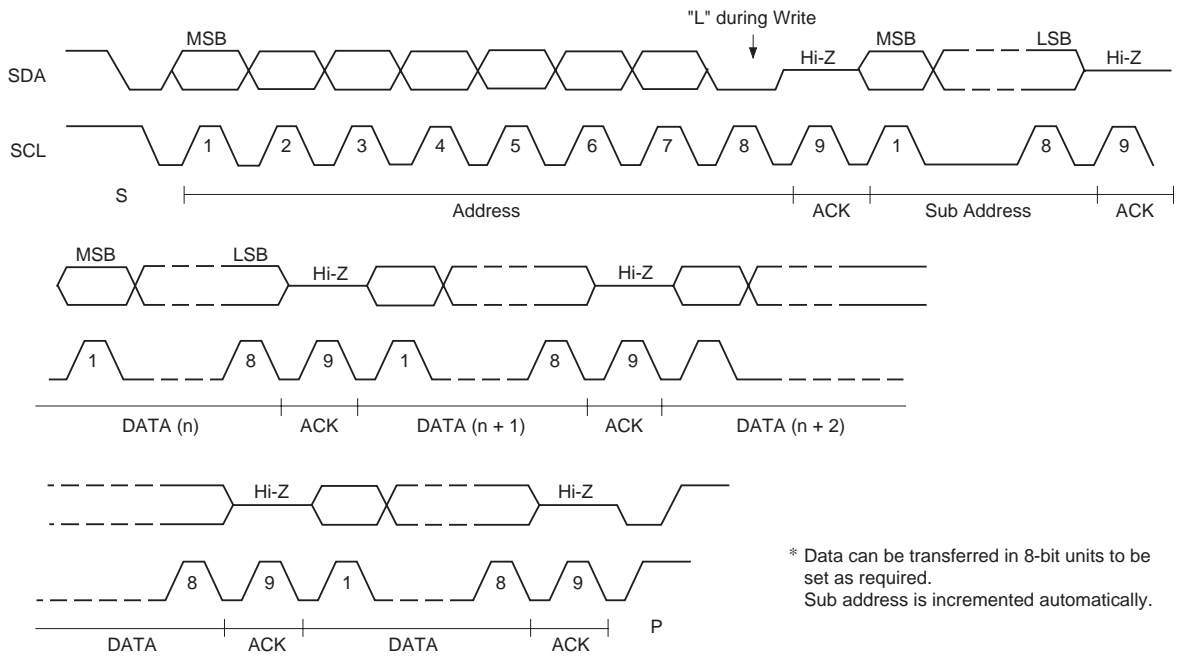
- ◆ Accordingly there are 3 values outputs, H, L and Hi-Z.



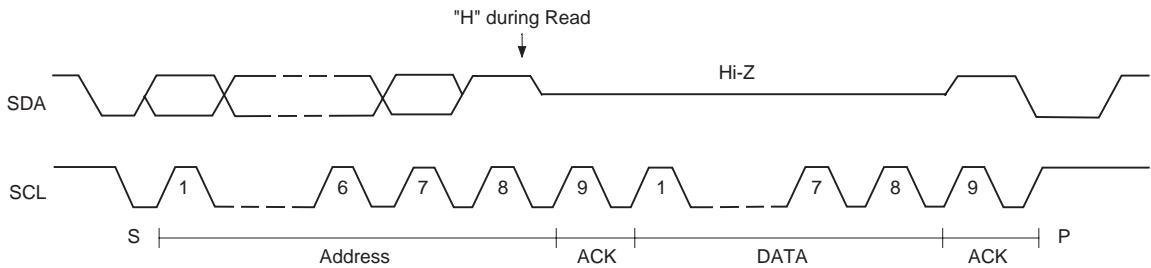
- ◆ I²C transfer begins with Start Condition and ends with Stop Condition.



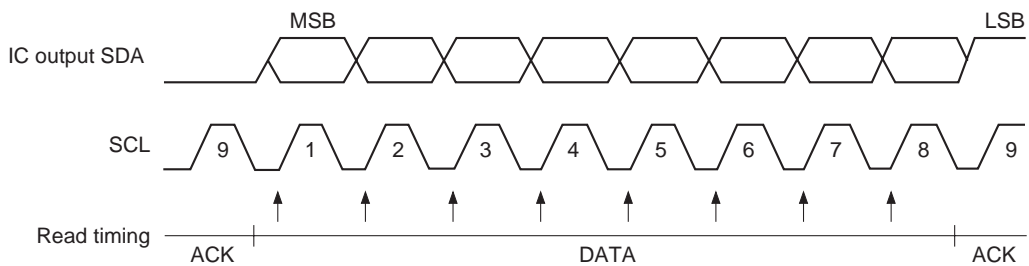
◆ I²C data Write (Write from I²C controller to the IC)



◆ I²C data Read (Read from the IC to I²C controller)



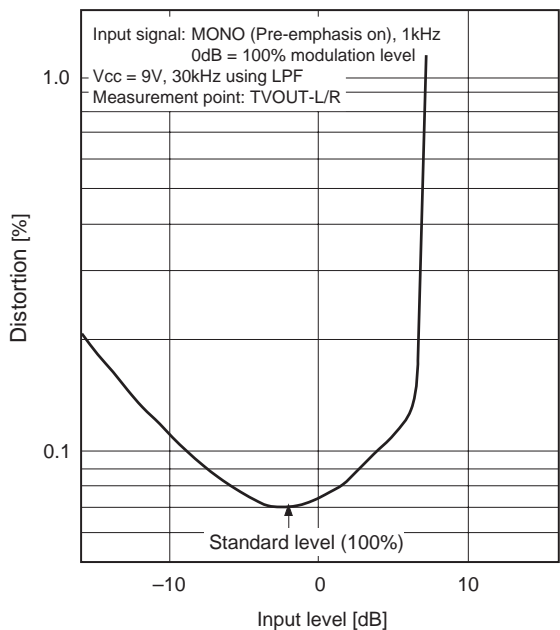
◆ Read timing



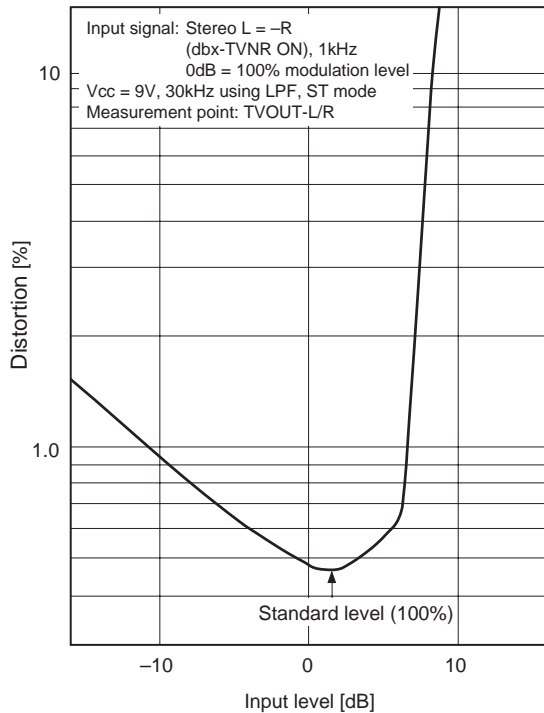
Note) Data Read is performed during SCL rise.

Example of Representative Characteristics

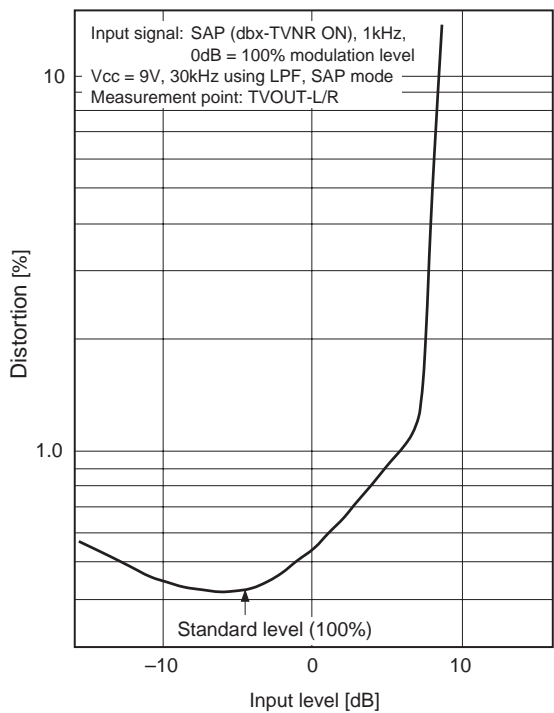
Input level vs. Distortion characteristics 1 (MONO)



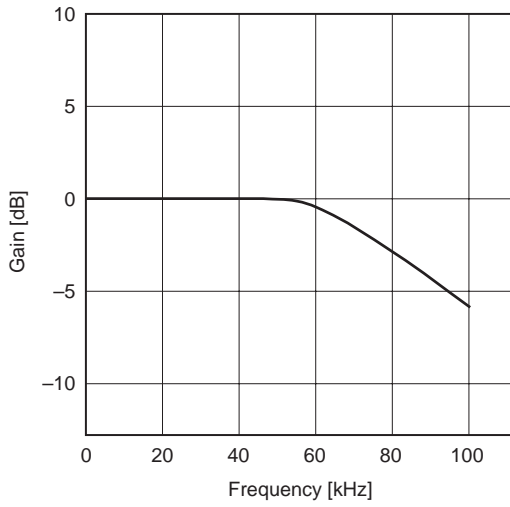
Input level vs. Distortion characteristics 2 (Stereo)



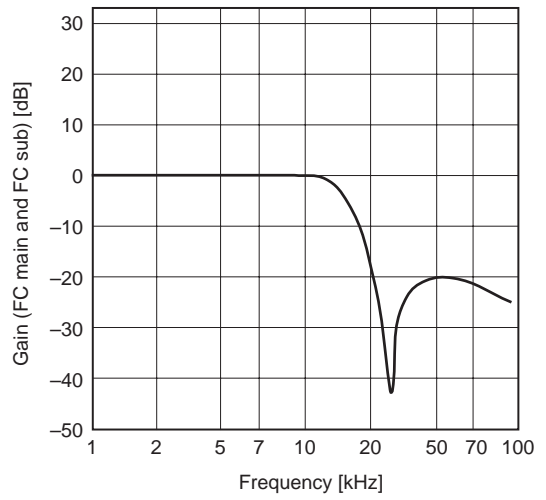
Input level vs. Distortion characteristics 3 (SAP)



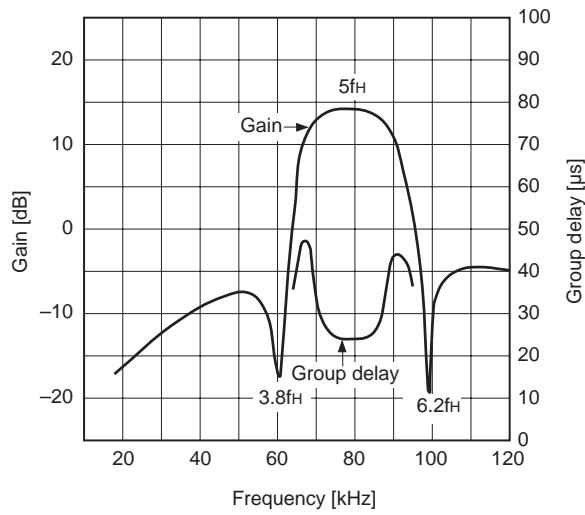
Stereo LPF frequency characteristics



Main LPF and Sub LPF frequency characteristics



SAP frequency characteristics and group delay



Additional SAP frequency characteristics

