

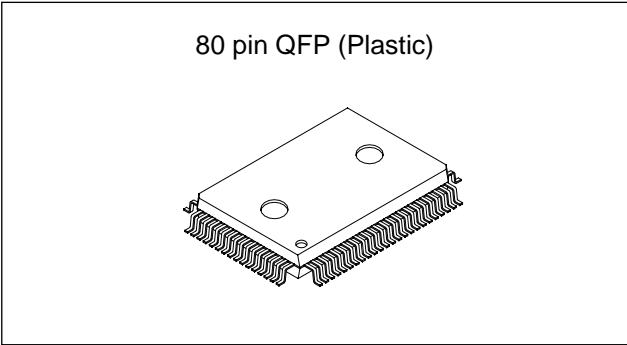
CMOS 8-bit Single Chip Microcomputer

Description

The CXP826P16 microcomputer is composed of a CPU, ROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, fluorescent display controller/driver, remote control receiver and 32kHz timer/counter.

This device also includes a power-on reset function and sleep/stop functions which can be used to achieve low power consumption.

The CXP826P16 is the PROM-incorporated version of the CXP82616 with built-in mask ROM, and it is able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



Features

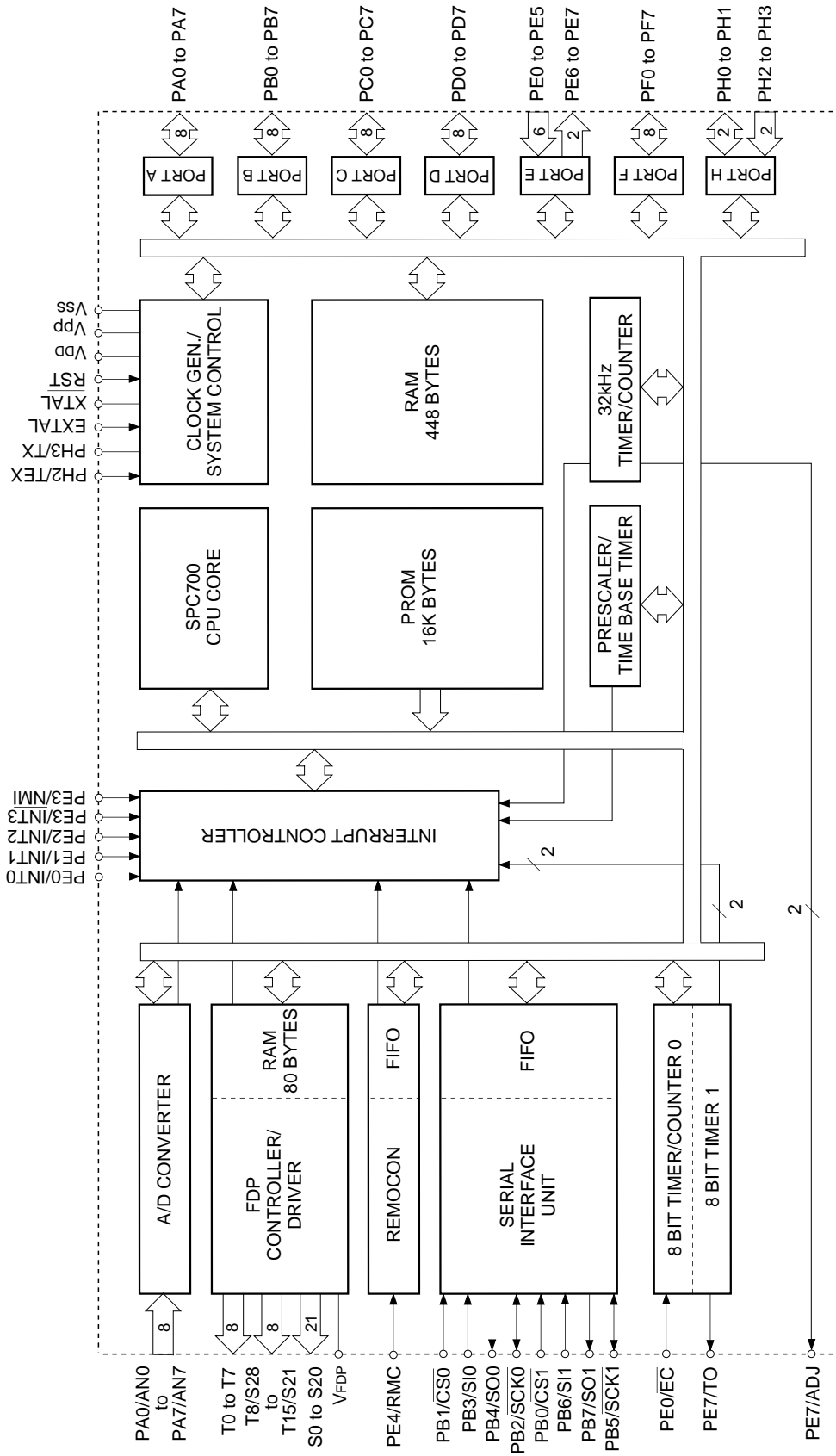
- Instruction set which supports a wide array of data types
 - 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
- Minimum instruction cycle 400ns for 10MHz, 122µs for 32kHz operation
- On-chip PROM 16K bytes
- On-chip RAM 448 bytes (Including fluorescent display data area)
- Peripheral functions
 - A/D converter 8-bit, 8-channel, successive approximation system (conversion rate 32µs/10MHz)
 - Serial interface On-chip 8-bit, 8-stage FIFO (1 to 8 bytes auto transfer), 1 circuit 2-channel
 - Timers 8-bit timer
8-bit timer/counter
19-bit time base timer
32kHz timer/counter
 - Fluorescent display controller/driver Maximum of 336 segments display available
1 to 16 digits dynamic display
Dimmer function
High voltage tolerance output (40V)
On-chip pull-down resistor (Mask option)
Hardware key scan function (Maximum of 8 x 16 key matrix available)
- Remote control receiver circuit On-chip 6-stage FIFO 8-bit pulse measurement counter
- Interrupts 13 factors, 13 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 80-pin plastic QFP

Structure

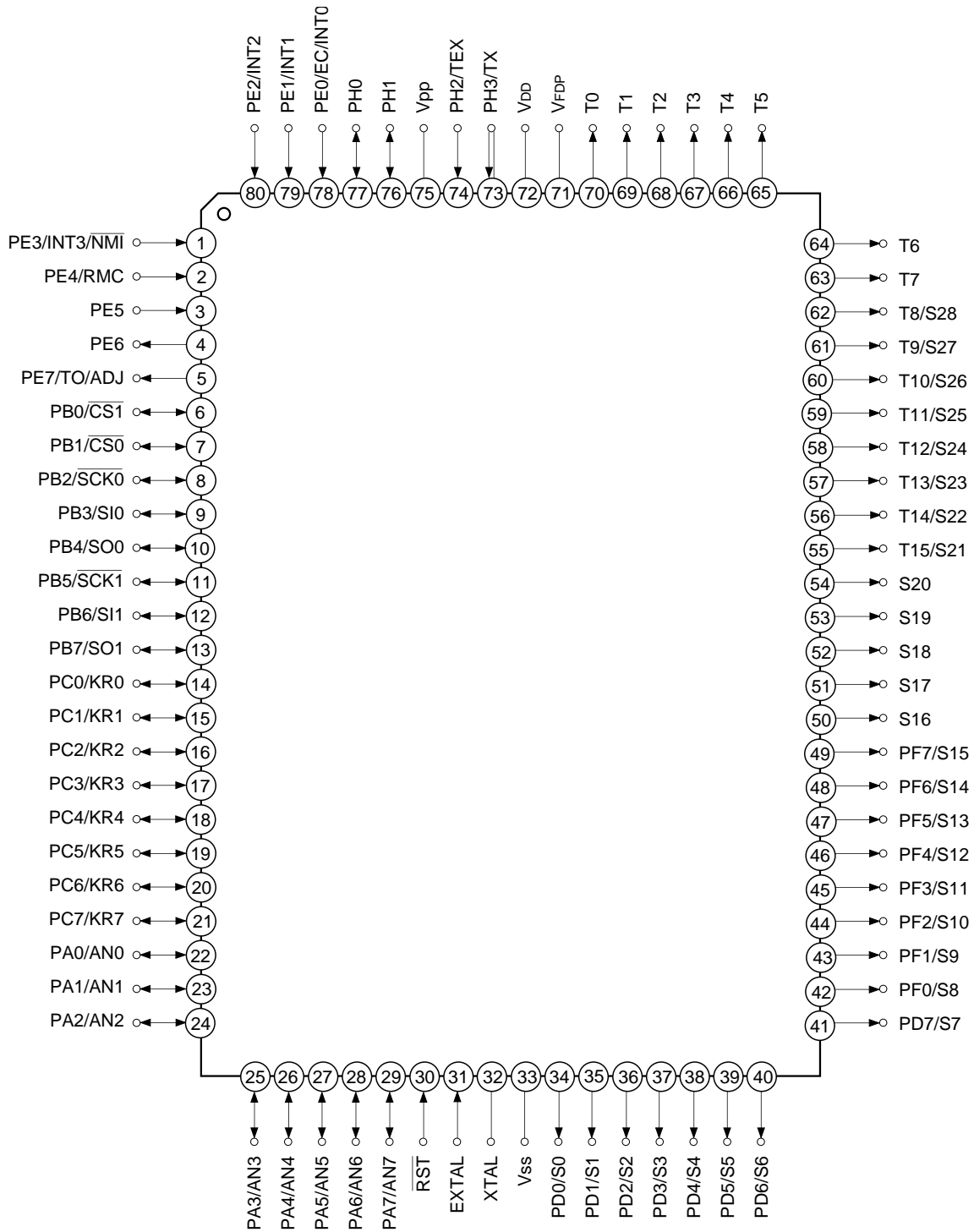
Silicon gate CMOS IC

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Block Diagram



Pin Assignment (Top View)



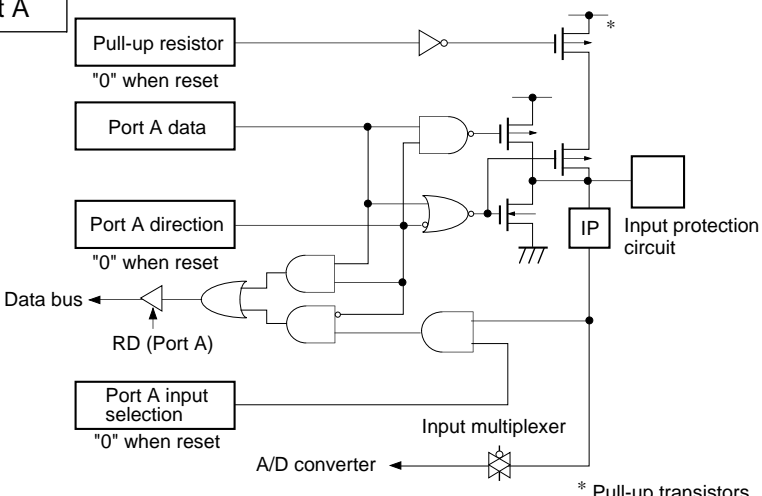
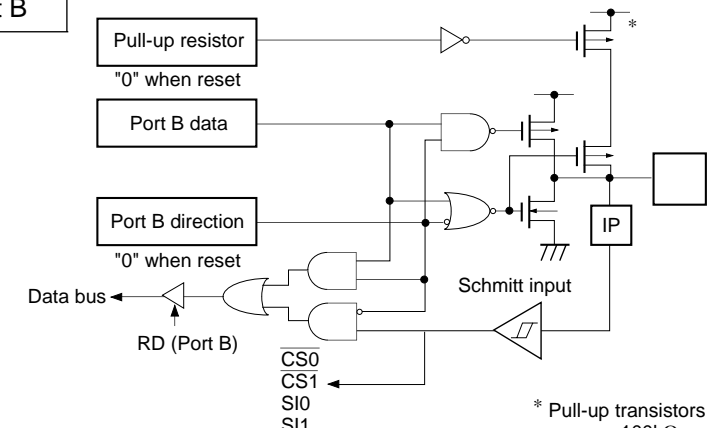
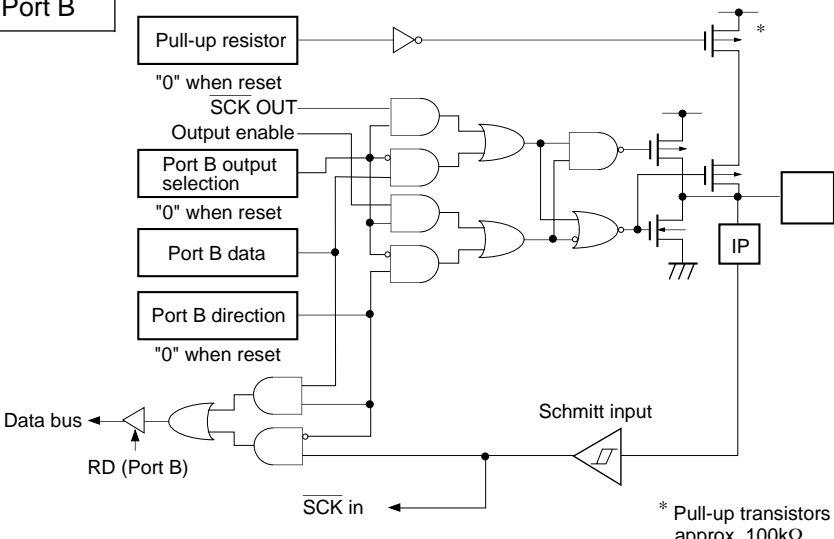
- Note)**
1. Vpp (Pin 75) is always connected to VDD.
 2. PH3/TX (Pin 73) is input port during port selection;
oscillation output during oscillation selection

Pin Description

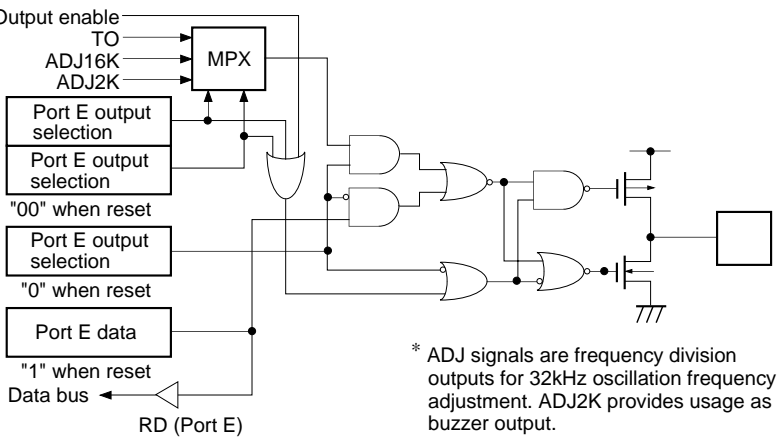
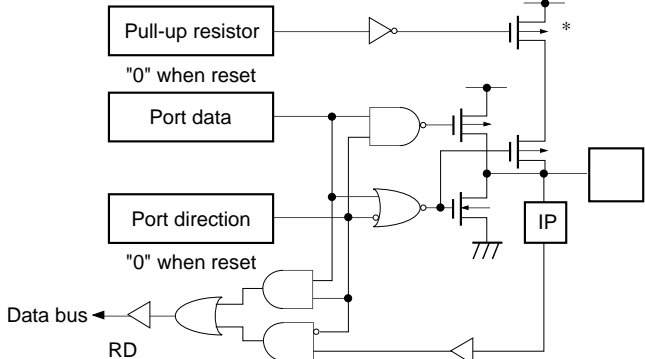
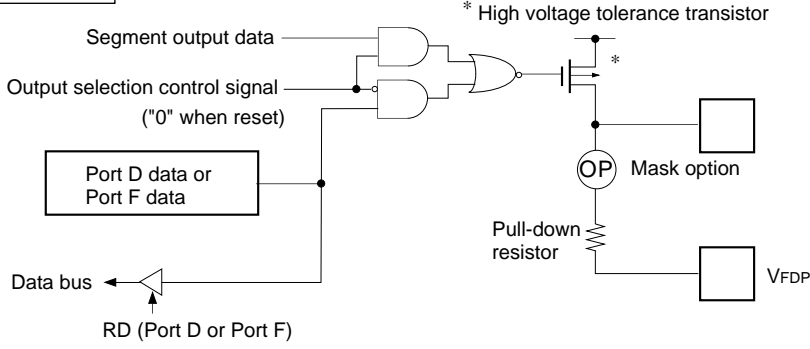
Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/ $\overline{CS1}$	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/ $\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a bit unit. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Key return input for FDP segment signal which performs key scanning.
PE0/INT0/ $\overline{EC0}$	Input/Input/ Input	(Port E) 8-bit port. Upper 6 bits are for inputs; lower 2 bits are for outputs. (8 pins)	External event input to timer/counter. (1 pin)
PE1/INT1	Input/Input		External interrupt request inputs. (4 pins)
PE2/INT2	Input/Input		
PE3/INT3/ \overline{NMI}	Input/Input/ Input		Non-maskable interruption request input.
PE4/RMC	Input/Input		Input for remote control receiver circuit.
PE5	Input		Output for timer/counter rectangular waveform and 32kHz oscillation frequency division.
PE6	Input		
PE7/TO/ ADJ	Output/Output		

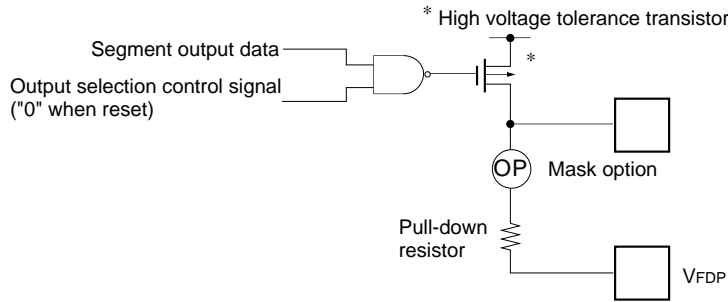
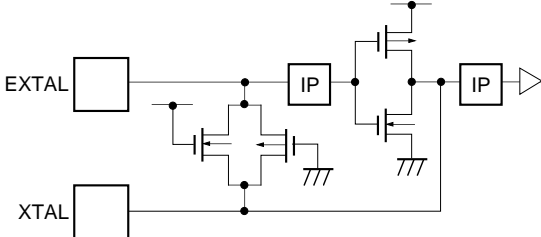
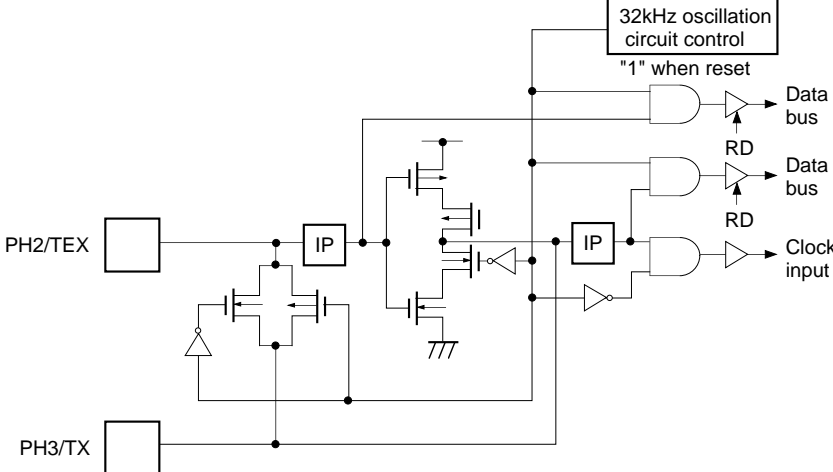
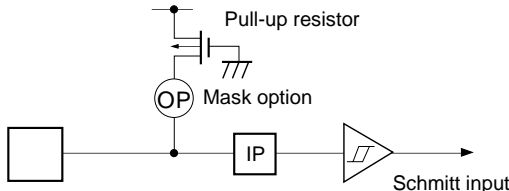
Symbol	I/O	Functions	
PH0 to PH1	I/O	(Port H) 2-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 2 bits. (2 pins)	
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit output port. (8 pins)	Segment signal output for FDP.
S16 to S20	Output	Segment signal output for FDP.	
T8/S28 to T15/S21	Output/Output	Output for FDP timing and segment signals.	
T0 to T7	Output	Timing signal output for FDP.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	Segment signal output for FDP.
V _{FDP}		Provides voltage for FDP when on-chip resistor is selected under mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
PH2/TEX	Input/Input	(Port H) 2-bit input port. (2 pins)	Crystal connectors for 32kHz timer/counter clock oscillation circuit. Connect a 32kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and leave TX open.
PH3/TX	Input/Output		
$\overline{\text{RST}}$	Input	Low-level active. System reset. $\overline{\text{RST}}$ is input pin.	
V _{pp}		Positive power supply pin for writing of built-in PROM. Under normal operating conditions, connect to V _{DD} .	
V _{DD}		V _{CC} supply.	
V _{SS}		GND	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB0/$\overline{\text{CS1}}$ PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 100kΩ</p> <p>SI0 and SI1 are not schmitt input.</p>	<p>Hi-Z</p>
<p>PB2/$\overline{\text{SCK0}}$ PB5/$\overline{\text{SCK1}}$</p> <p>2 pins</p>	<p>Port B</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PC0/KR0 to PC7/KR7</p> <p>8 pins</p>	<p>Port C</p> <p>*1 Large current drive of 12mA possible *2 Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PE0/\overline{EC}/INT0 PE1/INT1 PE2/INT2 PE3/INT3/\overline{NMI} PE4/RMC</p> <p>5 pins</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE5</p> <p>1 pin</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE6</p> <p>1 pin</p>	<p>Port E</p>	<p>High level</p>

Pin	Circuit format	When reset
<p>PE7/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>* ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p>	<p>High level (High level with 150kΩ resistor when reset)</p>
<p>PH0 to PH1</p> <p>2 pins</p>	<p>Port H</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PD0/S0 to PD7/S7</p> <p>PF0/S8 to PF7/S15</p> <p>16 pins</p>	<p>Port D</p> <p>Port F</p>  <p>* High voltage tolerance transistor</p> <p>Mask option</p> <p>V_{FDP}</p>	<p>Hi-Z or Low level (When PD resistor is connected)</p>

Pin	Circuit format	When reset
<p>S16 to S20 T15/S21 to T8/S28 T0 to T7</p> <p>21 pins</p>	 <p>* High voltage tolerance transistor</p> <p>Segment output data</p> <p>Output selection control signal ("0" when reset)</p> <p>Mask option</p> <p>Pull-down resistor</p> <p>VFDP</p>	<p>Hi-Z or Low level (When PD resistor is connected)</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit construction for oscillation. • During STOP feedback resistor is disconnected, and XTAL becomes "H" level. 	<p>Oscillation</p>
<p>PH2/TEX PH3/TX</p> <p>2 pins</p>	 <p>32kHz oscillation circuit control "1" when reset</p> <p>PH2/TEX</p> <p>PH3/TX</p> <p>Data bus</p> <p>RD</p> <p>Data bus</p> <p>RD</p> <p>Clock input</p>	<p>Oscillation halted port input</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
Display output voltage	V _{OD}	V _{DD} - 40 to V _{DD} + 0.3	V	As P channel transistor is open drain, V _{DD} voltage is determined as standard.
High level output current	I _{OH}	-5	mA	Other than display output pins* ² : per pin
	I _{ODH1}	-15	mA	Display output S0 to S20: per pin
	I _{ODH2}	-35	mA	Display output T0 to T7 T8/S28 to T15/S21: per pin
High level total output current	∑I _{OH}	-40	mA	Total of other than display output pins
	∑I _{ODH}	-100	mA	Total of display output pins
Low level output current	I _{OL}	15	mA	Port 1 pin
	I _{OLC}	20	mA	Large current port pin* ³
Low level total output current	∑I _{OL}	100	mA	Entire pin total
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*² Specifies output current of general-purpose I/O ports.

*³ The large current drive transistor is an N-ch transistor of Port C (PC).

Note) If the absolute maximum ratings are exceeded, the LSI could reach permanent breakdown. Also, observing recommended operating conditions is desirable; otherwise, the LSI's reliability could be affected.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High speed mode (1/2, 1/4 clock) guaranteed operation range
		3.5	5.5	V	Low speed mode (1/16 clock) guaranteed operation range
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold operation range during STOP
	V _{pp}	V _{pp} = V _{DD}		V	*4
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*1
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*2
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*3
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*1
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*2
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*3
Operating temperature	Topr	-10	+75	°C	

*1 All regular input port (PA, PB3, PB4, PB6, PB7, PC, PE5, PH).

*2 For pins \overline{RST} , $\overline{CS0}$, $\overline{CS1}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC}/INT0$, INT1, INT2, INT3/ \overline{NMI} , RMC.

*3 Specifies only for external clock input.

*4 V_{pp} should be the same voltage as V_{DD}.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA, PB, PC, PE6, PE7, PH0, PH1	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PA, PB, PC, PE6, PE7, PH0, PH1	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PC	VDD = 4.5V, IOL = 12.0mA			1.5	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IiLE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiHT	TEX	VDD = 5.5V, VIL = 5.5V	0.1		10	μA
	IiLT		VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
	IiLR	RST*1	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
	IiL	PA to PC*2, PH0*2, PH1*2		VDD = 4.5V, VIL = 4.0V	-3.3		
Display output current	IOH	S0 to S20	VDD = 4.5V VOH = VDD - 2.5V	-8			mA
		S21/T15 to S28/T8, T0 to T7		-20			mA
Open drain output leak current (P-CH Tr off state)	ILOL	S0 to S20, S21/T15 to S28/T8, T0 to T7	VDD = 5.5V, VOL = VDD - 35V, VFDP = VDD - 35V			-20	μA
Pull down resistor*3	RL	S0 to S20, S21/T15 to S28/T8, T0 to T7	VDD = 5V, VOD - VFDP = 30V	60	100	270	kΩ
Input/Output leak current	IIZ	PA to PC*2, PH0*2, PH1*2, RST*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA

Item	Symbol	Pin	Codition	Min.	Typ.	Max.	Unit
Supply current*4	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency divider clock)		20	40	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		400	1000	μA
	I _{DDS1}		Sleep mode		1.2	8	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DDS2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		9	30	μA
I _{DDS3}	Stop mode, V _{DD} = 5.5V, Termination of 10MHz and 32kHz crystal oscillation.				30	μA	
Input capacitance	C _{IN}	For pins other than S0 to S28, T0 to T7, PE6, PE7, V _{DD} , V _{SS} , V _{FDP}	1MHz clock 0V other than the measured pins		10	20	pF

- *1 $\overline{\text{RST}}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.
- *2 Pins PA to PC, PH0, and PH1 specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.
- *3 Applies when the on-chip pull-down resistor is selected under the mask option.
- *4 All output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall time	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	\overline{EC}	Fig. 3	t _{sys} + 50*			ns
Event count input clock rise and fall time	t _{ER} , t _{EF}	\overline{EC}	Fig. 3			20	ms
System clock frequency	fc	TEX TX	V _{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock application condition)		32.768		kHz
Event count input clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise and fall time	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE_H).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Fig. 1. Clock timing

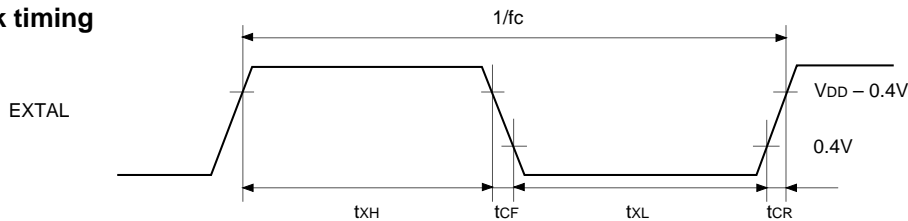


Fig. 2. Clock applied conditions

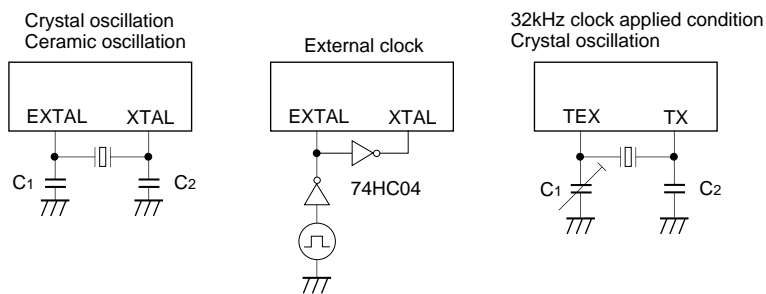
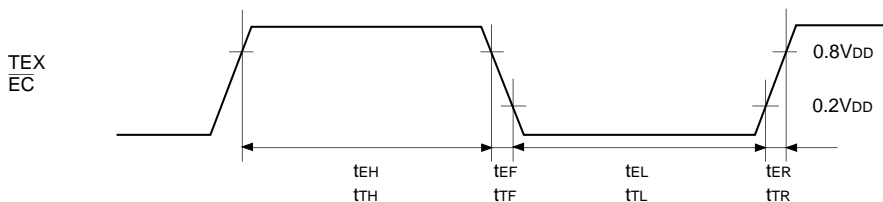


Fig. 3. Event count clock timing



(2) Serial transfer

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

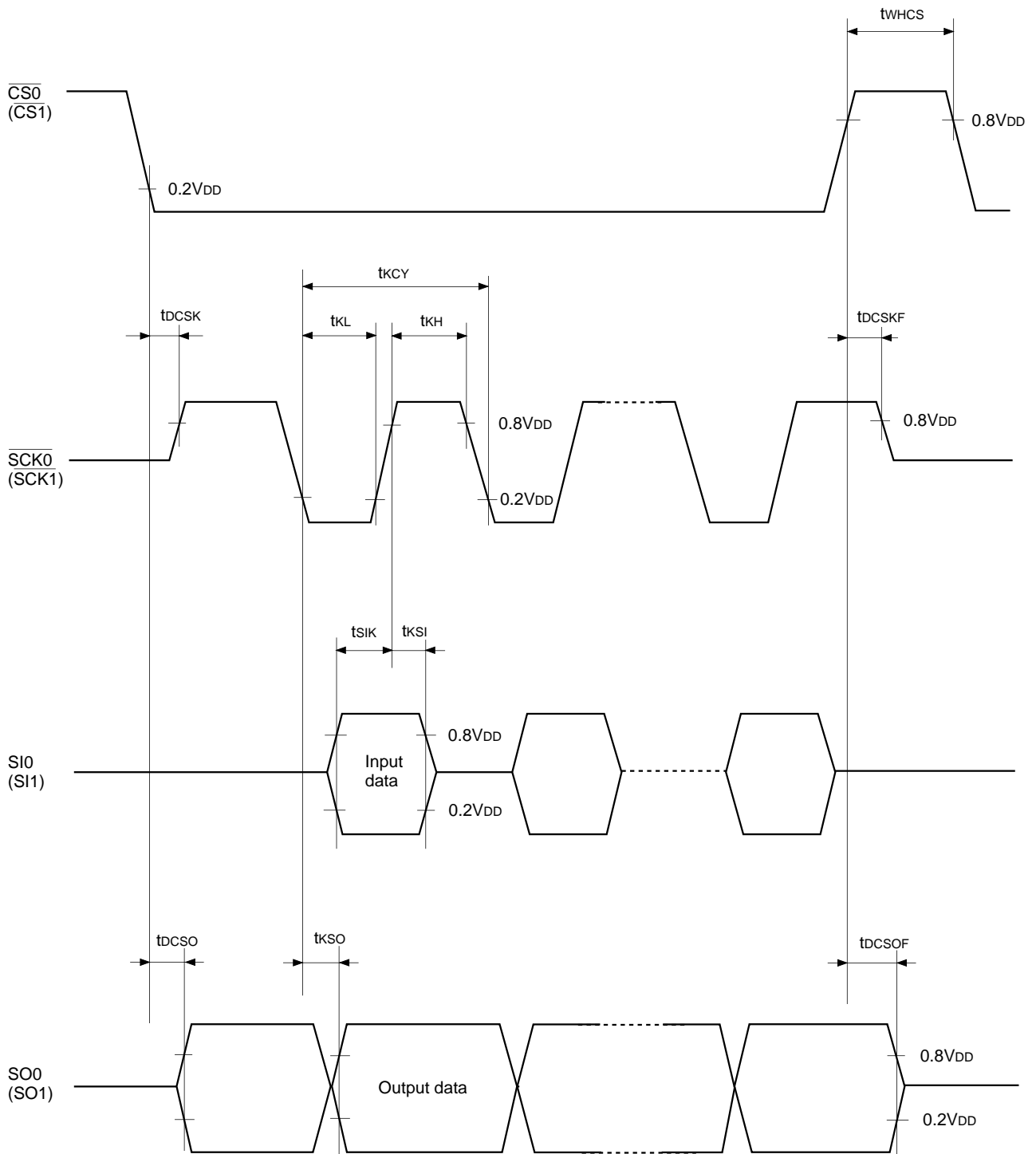
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \downarrow \rightarrow \overline{SCK1}$) delay time	t _{DCSK}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \uparrow \rightarrow \overline{SCK1}$) float delay time	t _{DCSKF}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		t _{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ ($\overline{CS1} \downarrow \rightarrow SO1$) delay time	t _{DCSO}	SO0 (SO1)	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ ($\overline{CS1} \uparrow \rightarrow SO1$) float delay time	t _{DCSOF}	SO0 (SO1)	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS0}$ ($\overline{CS1}$) high level width	t _{WHCS}	$\overline{CS0}$ ($\overline{CS1}$)	Chip select transfer mode	t _{sys} + 200		ns
$\overline{SCK0}$ ($\overline{SCK1}$) cycle time	t _{KCY}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ ($\overline{SCK1}$) high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 50		ns
SI0 (SI1) input setup time (for $\overline{SCK0} \uparrow$ ($\overline{SCK1} \uparrow$))	t _{SIK}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	100		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	200		ns
SI0 (SI1) input hold time (for $\overline{SCK0} \uparrow$ ($\overline{SCK1} \uparrow$))	t _{KSI}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	t _{sys} + 200		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ ($\overline{SCK1} \downarrow \rightarrow SO1$) delay time	t _{KSO}	SO0 (SO1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode		t _{sys} + 200	ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FEH).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ ($\overline{SCK1}$) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

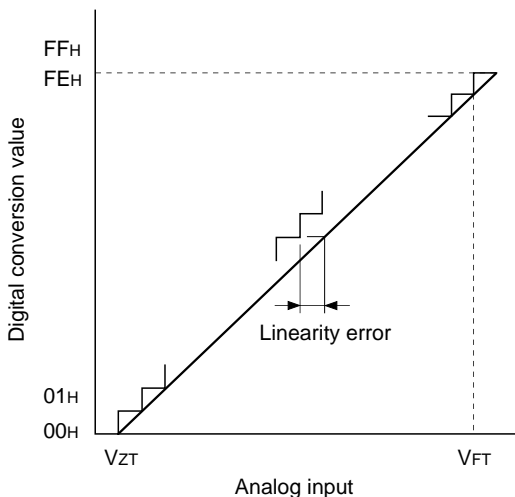


(3) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$			± 3	LSB
Zero transition voltage	V_{ZT}^{*1}			-10	10	70	mV
Full-scale transition voltage	V_{FT}^{*2}			4910	4970	5030	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Analog input voltage	V_{IAN}	AN0 to AN7		-0.3		$V_{DD} + 0.3$	V

Fig. 5. Definition of A/D converter terms



- *1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.
- *2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.
- *3 f_{ADC} indicates the below values due to the Bit6 (CKS) of A/D control register (address: 00F9H) and the Bit7 (PCK1) and Bit6 (PCK0) of clock control register (address: 00FEH)

PCK1, 0	CKS	
	0 ($\phi/2$ selection)	1 (ϕ selection)
00 ($\phi = f_{EX}/2$)	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ($\phi = f_{EX}/4$)	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ($\phi = f_{EX}/16$)	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input (Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t _{IH} t _{IL}	INT0 INT1 INT2 INT3 $\overline{\text{NMI}}$		1		μs
Reset input low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig 6. Interruption input timing

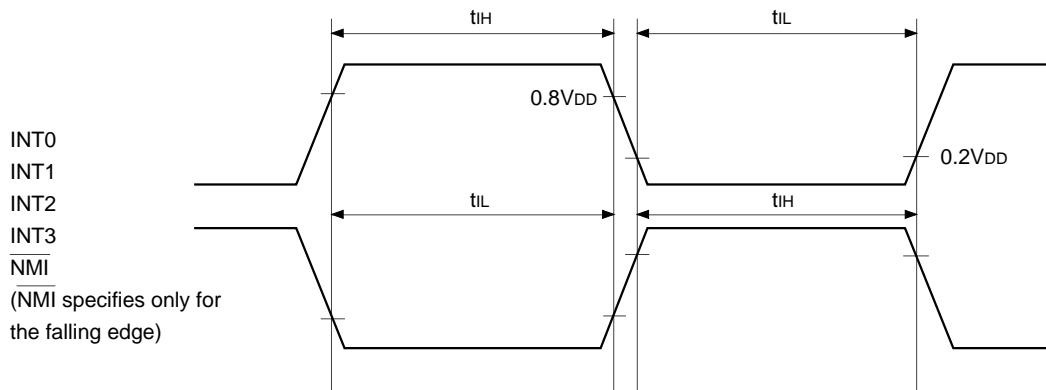
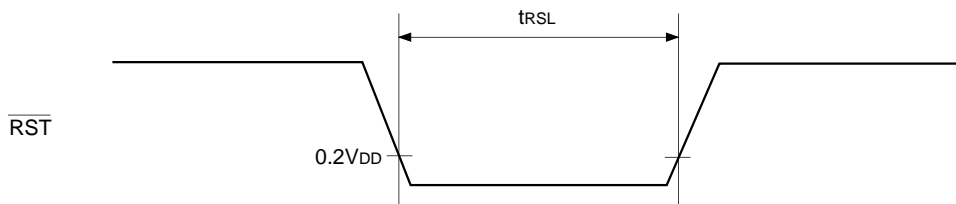
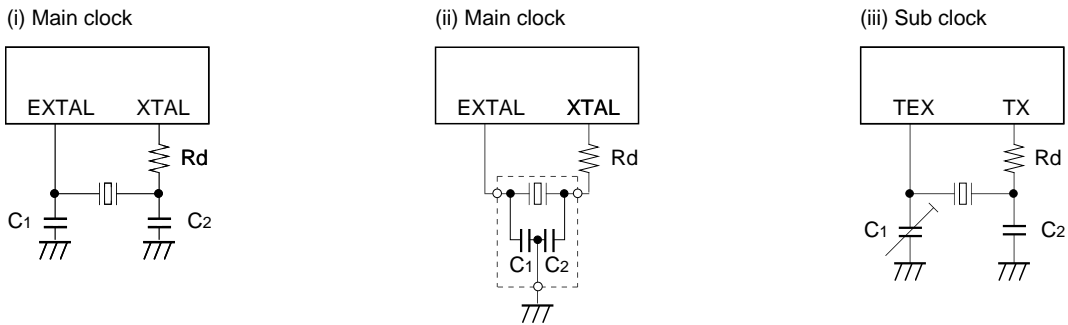


Fig. 7. $\overline{\text{RST}}$ input timing



Appendix

Fig. 8. Recommended oscillation circuit



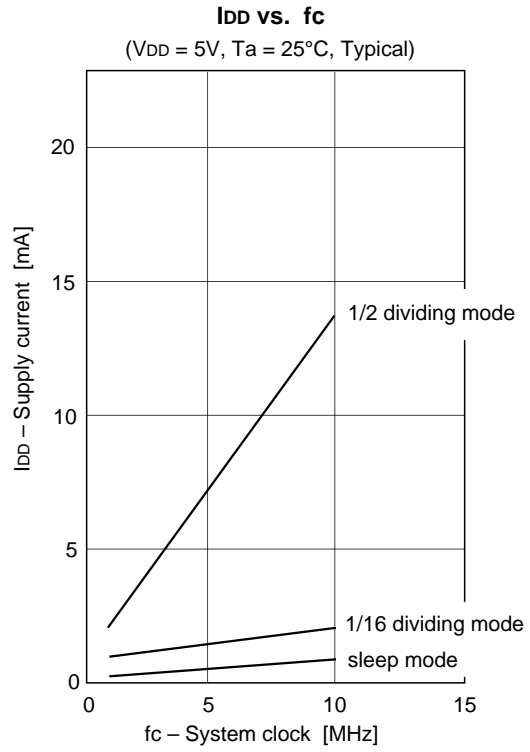
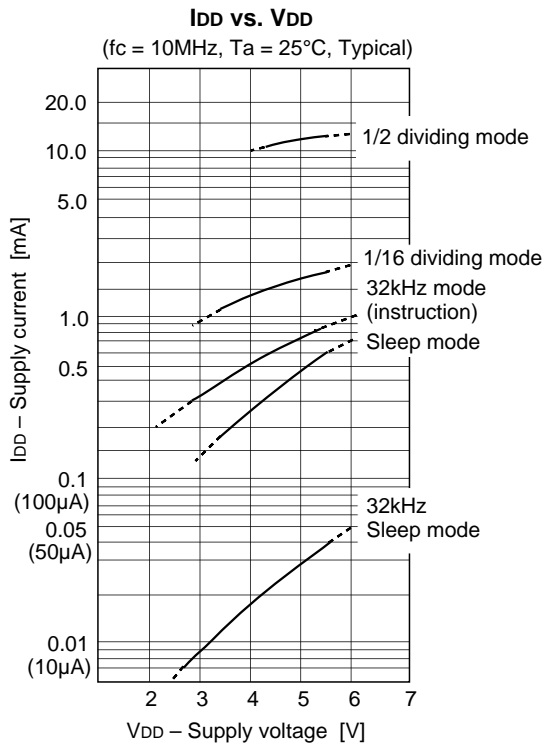
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

Selection Guide

Option Item	Mask Product	CXP826P16Q-1-□□□
Package	80-pin plastic QFP	80-pin plastic QFP
ROM capacitance	12Kbyte/16Kbyte	PROM 16Kbyte
Reset pin pull-up resistor	Existent/Non-Existent	Existent
High voltage drive output pin pull-down resistor	Existent/Non-Existent	Non-Existent (PD0/S0 to PF7/S15) Existent (T0 to S16)

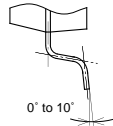
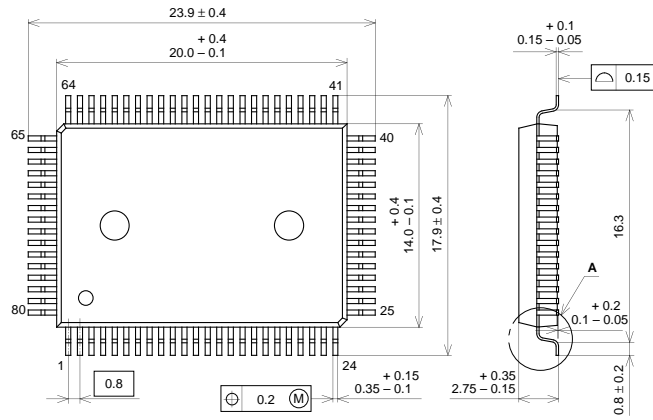
Characteristics Curves



Package Outline

Unit : mm

80PIN QFP (PLASTIC)



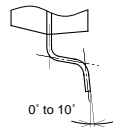
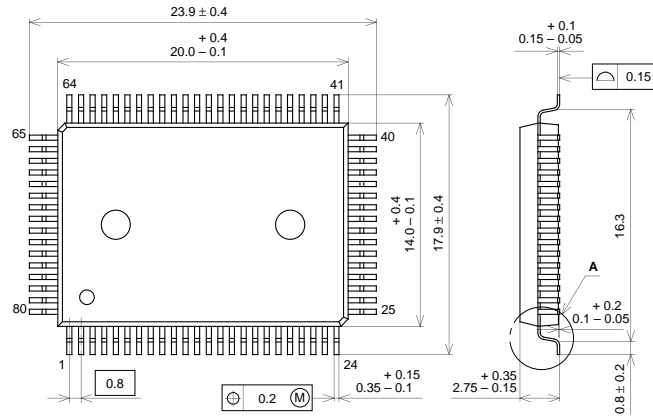
DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm