

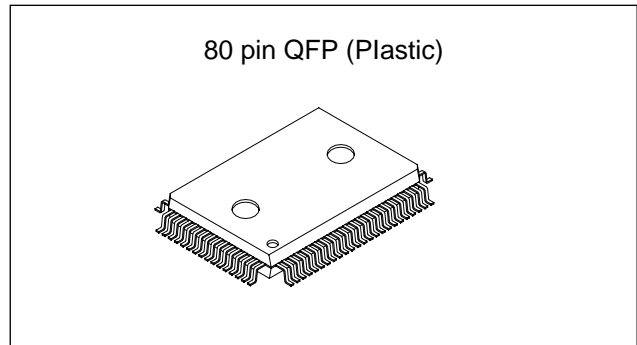
## CMOS 8-bit Single Chip Microcomputer

### Description

The CXP844P16 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, 32kHz timer/counter, remote control reception circuit and other servo systems besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP844P16 also provides a sleep/stop function that enables lower power consumption.

This IC is the PROM-incorporated version of the CXP84416 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



### Features

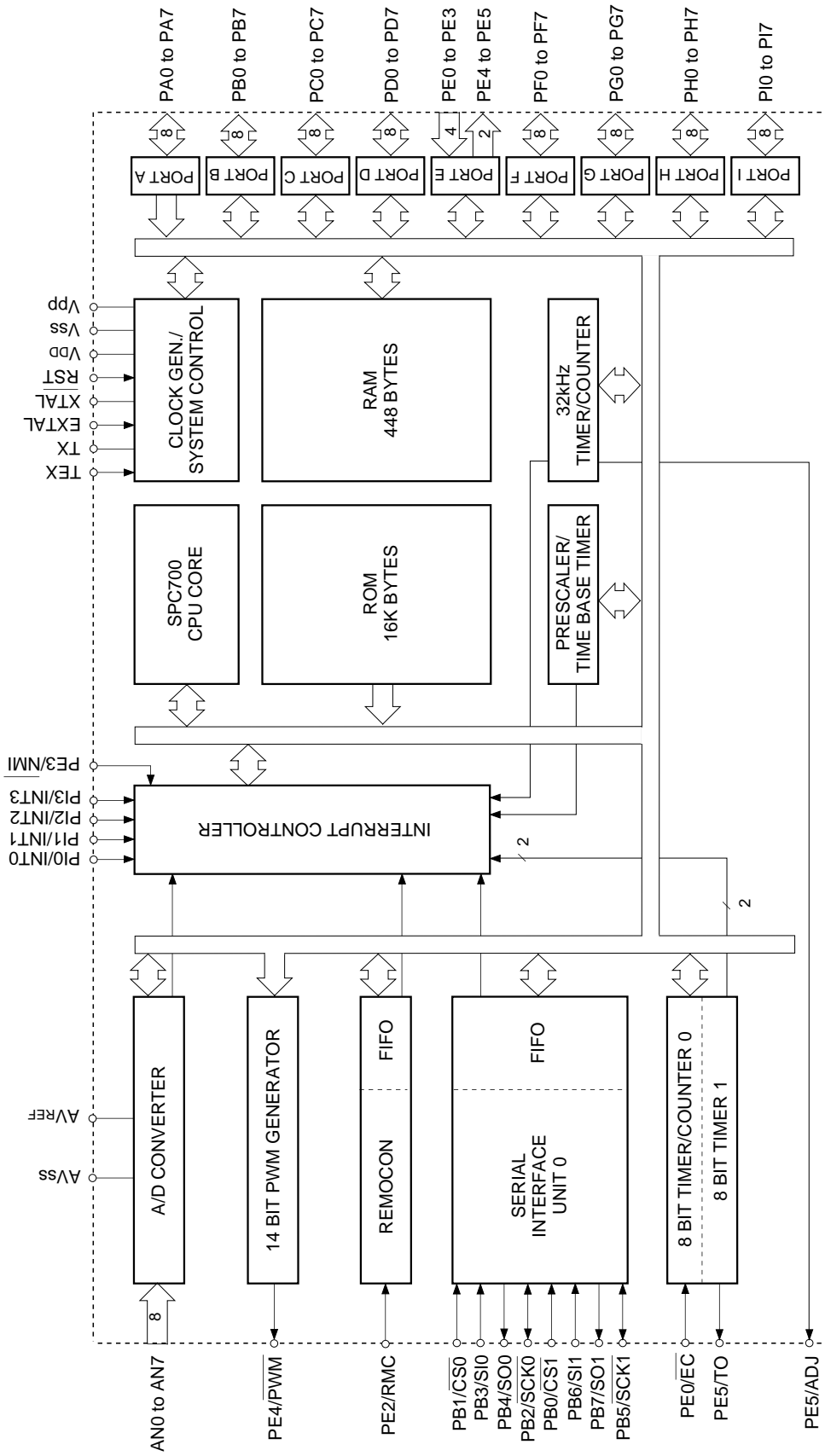
- Wide-range instruction system (213 instructions) to cover various types of data.
  - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
  - 400ns at 10MHz operation
  - 122µs at 32kHz operation
- Incorporated PROM capacity 16Kbytes
- Incorporated RAM capacity 448bytes
- Peripheral functions
  - A/D converter 8-bit, 8-channel, successive approximation method (Conversion time of 32µs/10MHz)
  - Serial interface Incorporated 8-bit, 8-stage FIFO (Auto transfer for 1 to 8 bytes), 2 channel
  - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
  - Remote control reception circuit Incorporated 6-stage FIFO 8-bit measurement counter
  - PWM output for tuner 14 bits, 1 channel
- Interruption 12 factors, 12 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 80-pin plastic QFP

### Structure

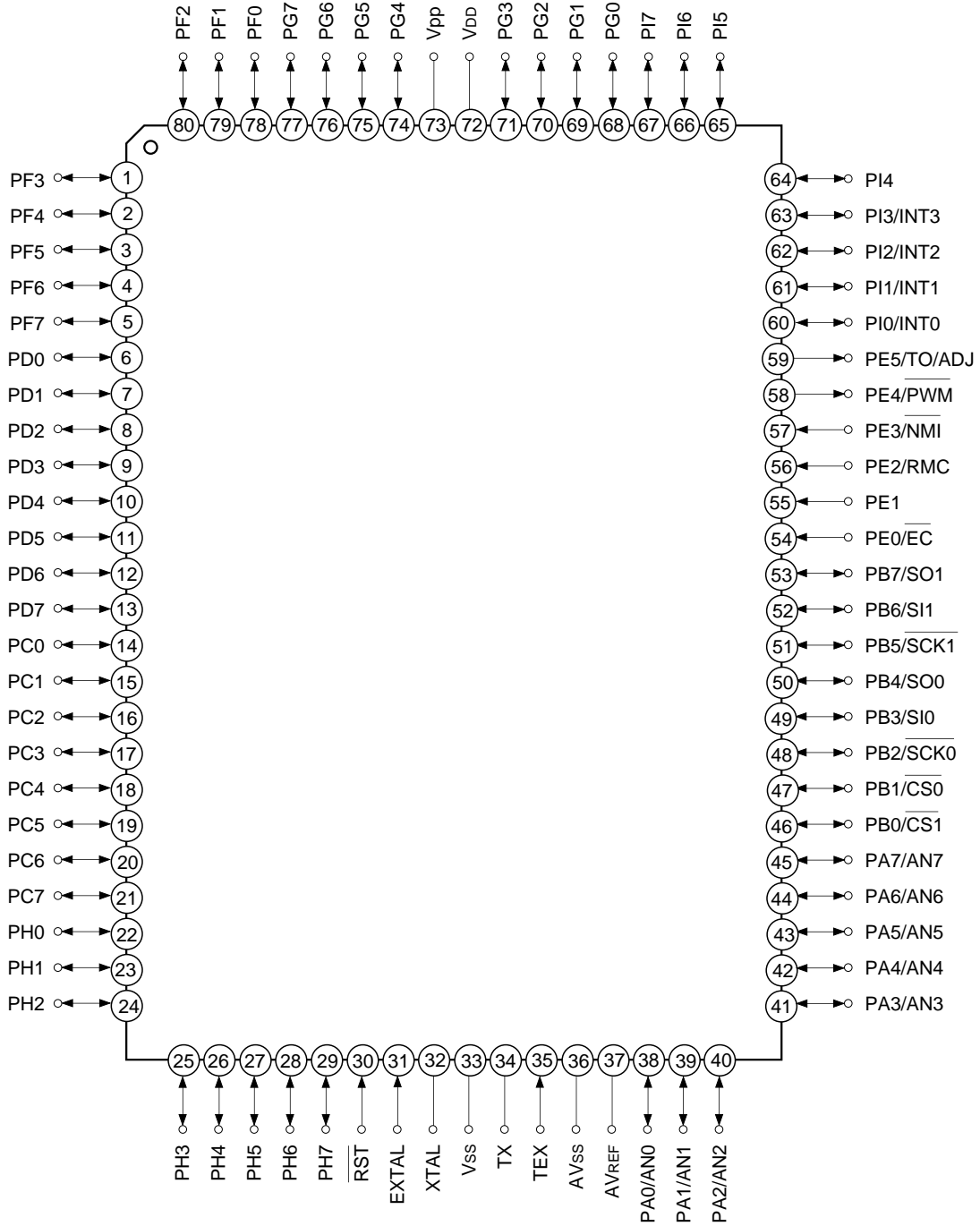
Silicon gate CMOS IC

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



Pin Assignment (Top View)



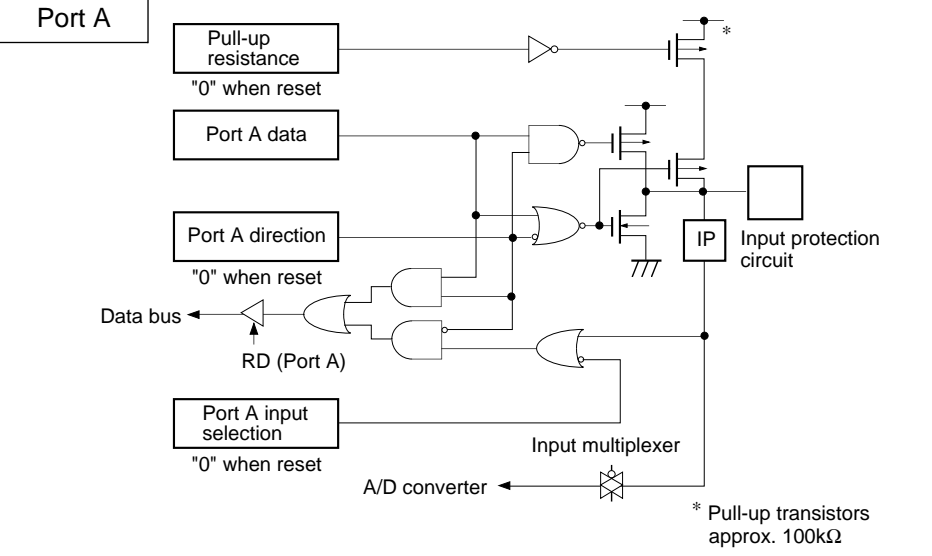
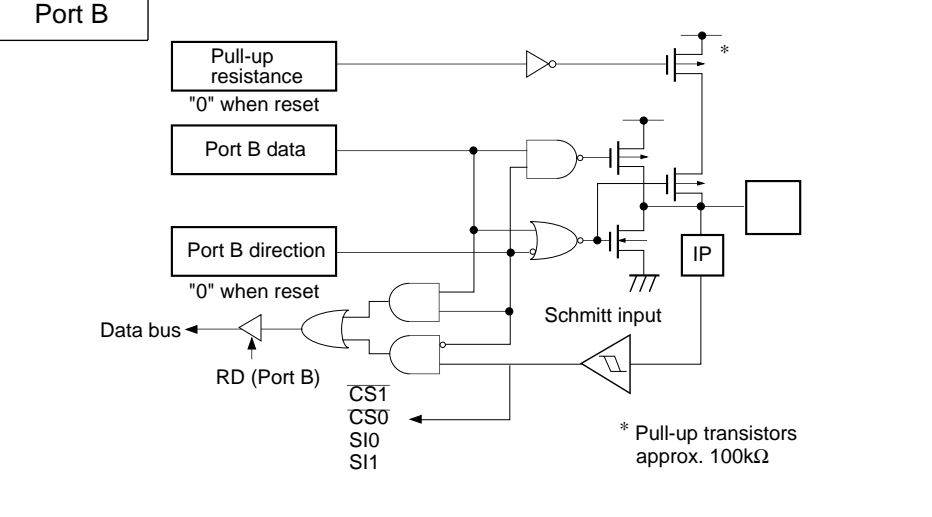
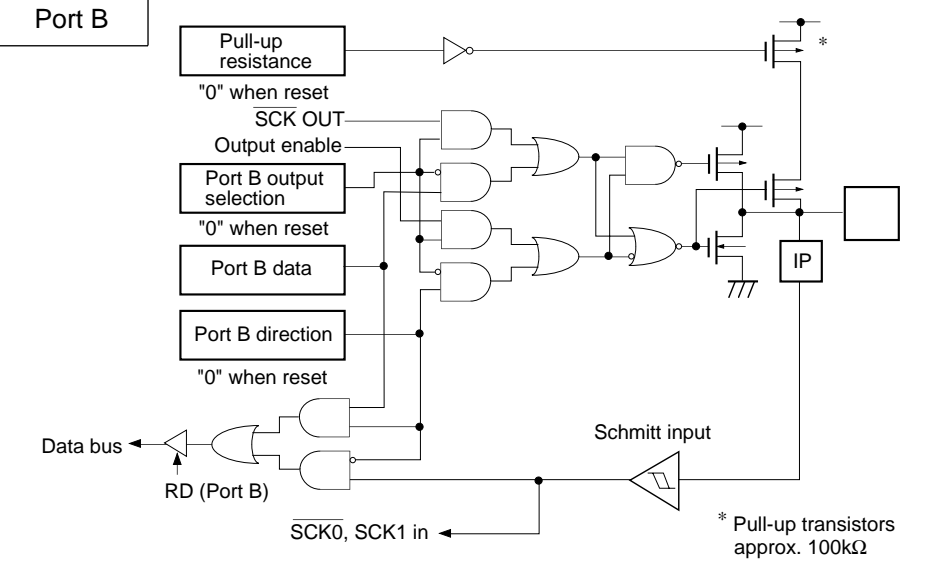
**Note)** NC (Pin 73) must be connected to VDD.

Pin Description

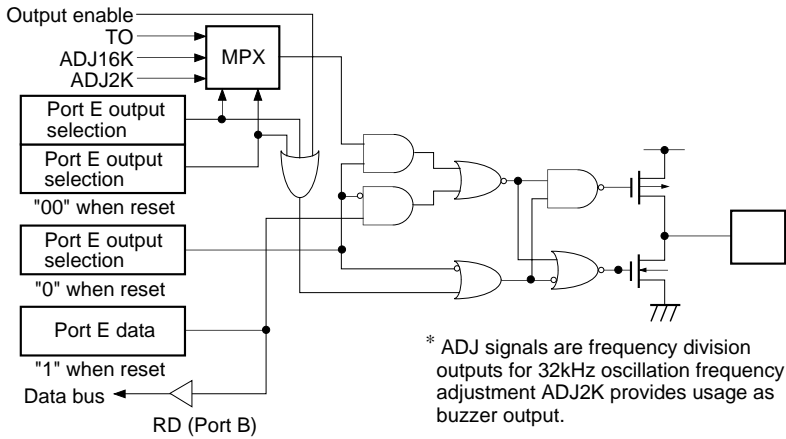
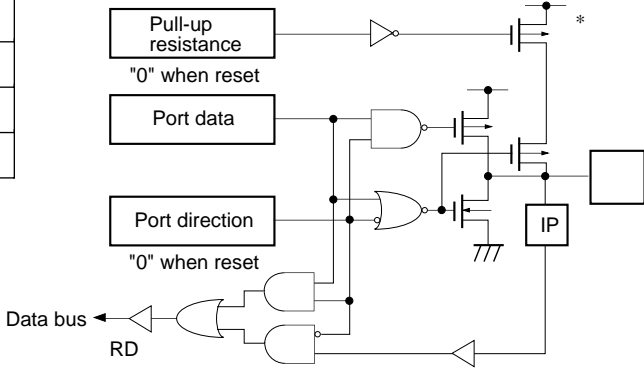
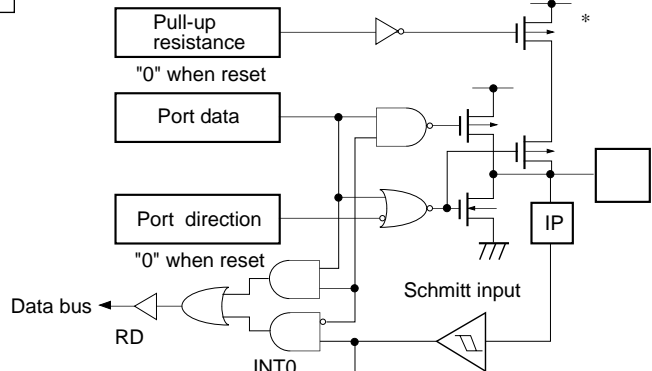
Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/analog input	(Port A) 8-bit I/O port. I/O can be set in single bit units. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/ $\overline{\text{CS1}}$	I/O/input	(Port B) 8-bit I/O port. I/O can be set in single bit units. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/ $\overline{\text{CS0}}$	I/O/input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/input		Serial data input (CH0).
PB4/SO0	I/O/output		Serial data output (CH0).
PB5/ $\overline{\text{SCK1}}$	I/O/input/output		Serial clock I/O (CH1).
PB6/SI1	I/O/input		Serial data input (CH1).
PB7/SO1	I/O/output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/ $\overline{\text{EC}}$	Input/input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. Incorporation of pull-up resistor can be set through the software. (8 pins)	External event inputs for timer/counter.
PE1	Input		
PE2/RMC	Input/input		Remote control reception circuit input.
PE3/ $\overline{\text{NMI}}$	Input/input		Non-maskable interruption request input.
PE4/ $\overline{\text{PWM}}$	Output/output		14-bit PWM output.
PE5/ $\overline{\text{TO/ADJ}}$	Output/output/ output		Rectangular wave output for 16-bit timer/counter (duty output 50%). Output for 32kHz oscillation frequency demultiplication.
PF0 to PF7	I/O	(Port F) 8-bit output port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

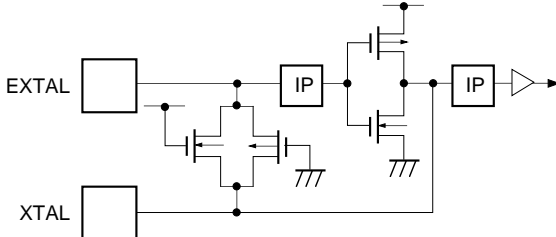
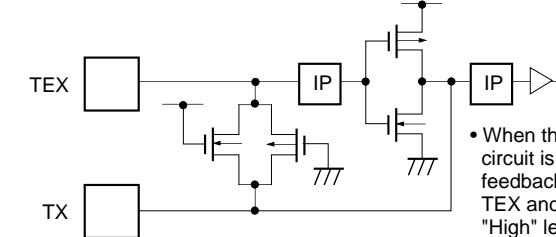
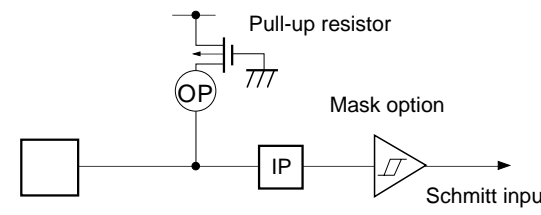
Pin code	I/O	Functions	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/input	(Port I) 8-bit output ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs.
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. Connect a 32.768kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
Vpp		Vcc supply for writing of built-in PROM. Under normal operating conditions, connect to VDD.	
AVREF	Input	Reference voltage input for A/D converter.	
AVss		A/D converter GND.	
VDD		Vcc supply.	
Vss		GND	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p>  <p>Pull-up resistance "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>IP Input protection circuit</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB0/<math>\overline{\text{CS1}}</math> PB1/<math>\overline{\text{CS0}}</math> PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p>  <p>Pull-up resistance "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>CS1 CS0 SI0 SI1</p> <p>IP</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB2/<math>\overline{\text{SCK0}}</math> PB5/<math>\overline{\text{SCK1}}</math></p> <p>2 pins</p>	<p>Port B</p>  <p>Pull-up resistance "0" when reset</p> <p>SCK OUT</p> <p>Output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>Schmitt input</p> <p>SCK0, SCK1 in</p> <p>IP</p> <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1  2 pins	<p>Port B</p> <p>* Pull-up transistors approx. 100kΩ</p>	Hi-Z
PC0 to PC7  8 pins	<p>Port C</p> <p>*1 High current drive of 12mA possible      *2 Pull-up transistors approx. 100kΩ</p>	Hi-Z
PE0/ $\overline{EC}$ PE1 PE2/RMC PE3/NMI  4 pins	<p>Port E</p> <p>Note : PE1 No schmitt input.</p>	Hi-Z
PE4/ $\overline{PWM}$  1 pin	<p>Port E</p>	H level

Pin	Circuit format	When reset
<p>PE5/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>* ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment ADJ2K provides usage as buzzer output.</p>	<p>H level</p> <p>When reset. "H level" with about 150kΩ resistor.</p>
<p>PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7</p> <p>36 pins</p>	<p>Port D</p> <p>Port F</p> <p>Port G</p> <p>Port H</p> <p>Port I</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PI0 to PI3</p> <p>4 pins</p>	<p>Port I</p>  <p>* Pull-up transistors approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop and XTAL becomes "High" level.</li> </ul>	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p>	<p>L level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13.0	V	Incorporated PROM
	AV <sub>SS</sub>	-0.3 to +0.3	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
High level output current	I <sub>OH</sub>	-5	mA	Output per pin
High level total output current	∑I <sub>OH</sub>	-50	mA	Total for all output pins
Low level output current	I <sub>OL</sub>	15	mA	Value per pin, excluding high current outputs
	I <sub>OLC</sub>	20	mA	Value per pin* <sup>2</sup> for high current outputs
Low level total output current	∑I <sub>OL</sub>	100	mA	Total for all output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> The high current drive transistor is the N-ch transistor of Port C (PC)

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	High speed mode guaranteed operation range* <sup>1</sup>
		3.5	5.5		Low speed mode guaranteed operation range* <sup>1</sup>
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
	V <sub>pp</sub>	V <sub>pp</sub> = V <sub>DD</sub>		V	* <sup>5</sup>
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	* <sup>2</sup>
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	Hysteresis input* <sup>3</sup>
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL* <sup>4</sup>
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	* <sup>2</sup>
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	Hysteresis input* <sup>3</sup>
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL* <sup>4</sup>
Operating temperature	T <sub>opr</sub>	-10	+75	°C	

\*<sup>1</sup> High speed mode is 1/2 frequency demultiplication clock selection; low-speed mode is 1/16 frequency demultiplication clock selection.

\*<sup>2</sup> Value for each pin of normal input ports (PA, PB4, PB7, PC, PD, PE1, PF to PH, PI4 to PI7).

\*<sup>3</sup> Value of the following pins:  $\overline{\text{RST}}$ ,  $\overline{\text{CS0}}$ ,  $\overline{\text{CS1}}$ ,  $\overline{\text{SCK0}}$ ,  $\overline{\text{SCK1}}$ , SI0, SI1,  $\overline{\text{EC}}$ , RMC,  $\overline{\text{NMI}}$ , INT0, INT1, INT2, INT3.

\*<sup>4</sup> Specifies only during external clock input.

\*<sup>5</sup> V<sub>pp</sub> and V<sub>DD</sub> should be set to same voltage.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	VOH	PA to PD, PE4, PE5, PF to PI	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output current	VOL		VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PC	VDD = 4.5V, IOL = 12.0mA			1.5	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IiLE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiHT	TEX	VDD = 5.5V, VIL = 5.5V	0.1		10	μA
	IiLT			-0.1		-10	μA
	IiLR	RST*1	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
	IiL	PA to PD*2, PF to PI*2	VDD = 4.5V, VIL = 4.0V	-3.3		-50	μA
I/O leakage current	IIZ	PE0 to PE3, RST*1, PA to PD*2, PF to PI*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Power supply current*3	IDD1	VDD	High-speed mode operation (1/2 frequency demultiplier clock)		18	40	mA
			VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)				
	IDD2		VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		400	1000	μA
	IDDS1		SLEEP mode		1.1	8	mA
			VDD = 5.5V, 10MHz crystal oscillation (C1 = C2 = 15pF)				
IDDS2	VDD = 3V, 32kHz crystal oscillation (C1 = C2 = 47pF)		9	30	μA		
IDDS3	STOP mode				30	μA	
		VDD = 5.5V, 10MHz crystal oscillation; and termination of 32kHz oscillation					
Input capacity	CIN	Pins other than PE4, PE5, XTAL, TX, AVREF, AVss, VDD, Vss	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

\*1 RST pin specifies the input current when the product with pull-up resistance has been selected, and specifies the leakage current when the product with no resistance has been selected. (Refer to the products list.)

\*2 Pins PA to PD, and PF to PI specifies the input current when pull-up resistance has been selected, and specifies the leakage current when no resistance has been selected.

\*3 When all pins are open.

**AC Characteristics**

**(1) Clock timing**

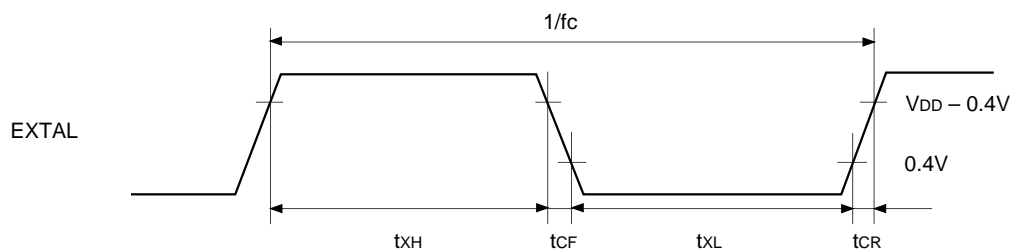
( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	$t_{XL}$ , $t_{XH}$	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	$t_{CR}$ , $t_{CF}$	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	$t_{EH}$ , $t_{EL}$	$\overline{\text{EC}}$	Fig. 3	$t_{\text{sys}} + 50^*$			ns
Event count input clock rise time, fall time	$t_{ER}$ , $t_{EF}$	$\overline{\text{EC}}$	Fig. 3			20	ms
System clock frequency	$f_c$	TEX TX	$V_{DD} = 2.7$ to $5.5\text{V}$ Fig. 2 (32kHz clock application condition)		32.768		kHz
Event count input clock input pulse width	$t_{TL}$ , $t_{TH}$	TEX	Fig. 3	10			$\mu\text{s}$
Event count input clock rise time, fall time	$t_{TR}$ , $t_{TF}$	TEX	Fig. 3			20	ms

\*  $t_{\text{sys}}$  indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FEH).

$t_{\text{sys}}$  (ns) = 2000/ $f_c$  (upper two bits = "00"), 4000/ $f_c$  (upper two bits = "01"), 16000/ $f_c$  (upper two bits = "11")

**Fig. 1. Clock timing**



**Fig. 2. Clock application conditions**

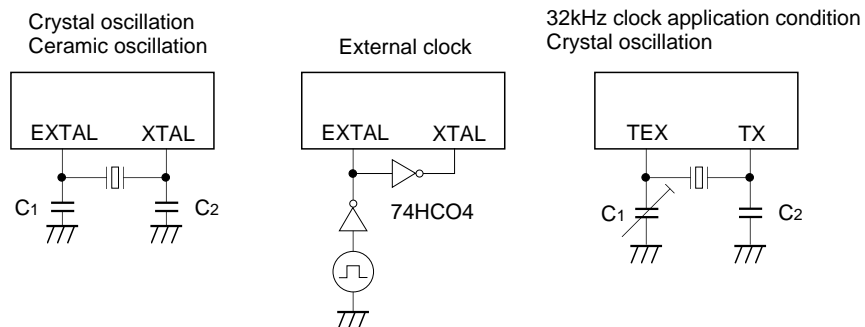
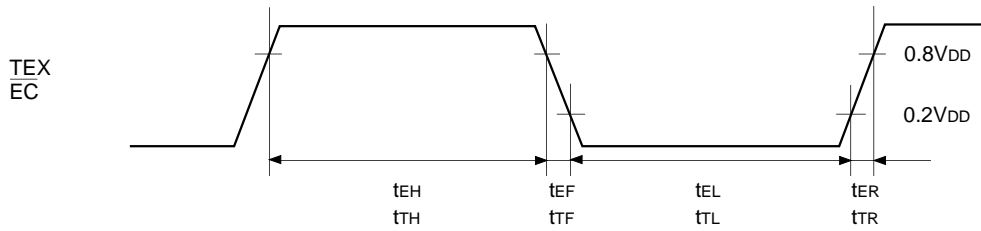


Fig. 3. Event count clock timing



(2) Serial transfer

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss reference)

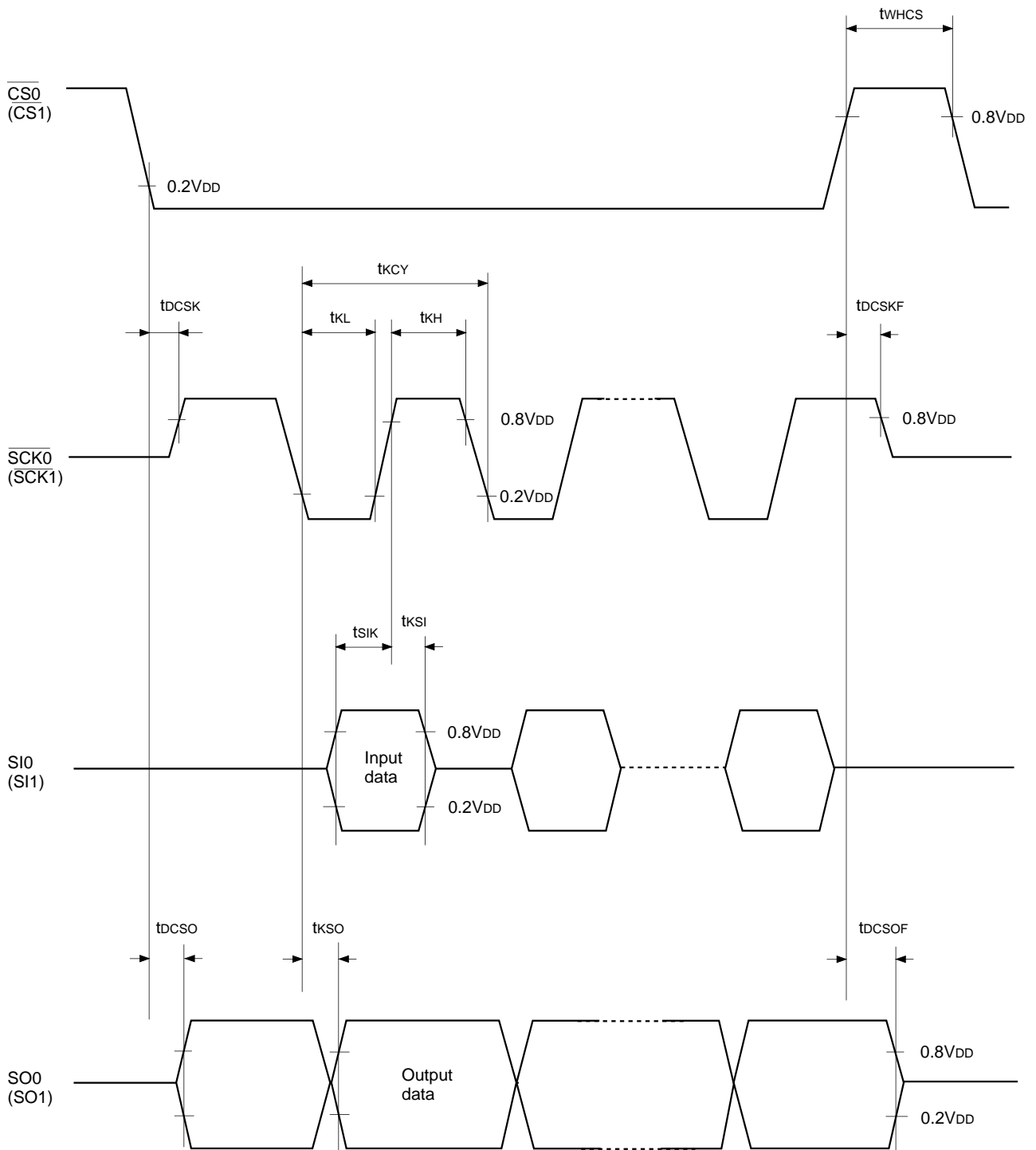
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ ( $\overline{CS1} \downarrow \rightarrow \overline{SCK1}$ ) delay time	$t_{DCSK}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Chip select transfer mode ( $\overline{SCK0}$ ( $\overline{SCK1}$ ) = output mode)		$1.5t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ ( $\overline{CS1} \uparrow \rightarrow \overline{SCK1}$ ) float delay time	$t_{DCSKF}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Chip select transfer mode ( $\overline{SCK0}$ ( $\overline{SCK1}$ ) = output mode)		$1.5t_{sys} + 200$	ns
$\overline{CS0} \downarrow \rightarrow SO0$ ( $\overline{CS1} \downarrow \rightarrow SO1$ ) delay time	$t_{DCSO}$	SO0 (SO1)	Chip select transfer mode		$1.5t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow SO0$ ( $\overline{CS1} \uparrow \rightarrow SO1$ ) float delay time	$t_{DCSOF}$	SO0 (SO1)	Chip select transfer mode		$1.5t_{sys} + 200$	ns
$\overline{CS0}$ ( $\overline{CS1}$ ) High level width	$t_{WHCS}$	$\overline{CS0}$ ( $\overline{CS1}$ )	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK0}$ ( $\overline{SCK1}$ ) cycle time	$t_{KCY}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Input mode	$2t_{sys} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{SCK0}$ ( $\overline{SCK1}$ ) High, Low level width	$t_{KH}$ $t_{KL}$	$\overline{SCK0}$ ( $\overline{SCK1}$ )	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI0 (SI1) input set-up time (for $\overline{SCK0} \uparrow$ )	$t_{SIK}$	SI0 (SI1)	$\overline{SCK0}$ ( $\overline{SCK1}$ ) input mode	100		ns
			$\overline{SCK0}$ ( $\overline{SCK1}$ ) output mode	200		ns
SI0 (SI1) input hold time (for $\overline{SCK0} \uparrow$ ( $\overline{SCK1} \uparrow$ ))	$t_{KSI}$	SI0 (SI1)	$\overline{SCK0}$ ( $\overline{SCK1}$ ) input mode	$t_{sys} + 200$		ns
			$\overline{SCK0}$ ( $\overline{SCK1}$ ) output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ ( $\overline{SCK1} \downarrow \rightarrow SO1$ ) delay time	$t_{KSO}$	SO0 (SO1)	$\overline{SCK0}$ ( $\overline{SCK1}$ ) input mode		$t_{sys} + 200$	ns
			$\overline{SCK0}$ ( $\overline{SCK1}$ ) output mode		100	ns

**Note 1)**  $t_{sys}$  indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FEH).

$t_{sys}$  (ns) = 2000/ $f_c$  (upper two bits = "00"), 4000/ $f_c$  (upper two bits = "01"), 16000/ $f_c$  (upper two bits = "11")

**Note 2)** The load condition for the  $\overline{SCK0}$  ( $\overline{SCK1}$ ) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

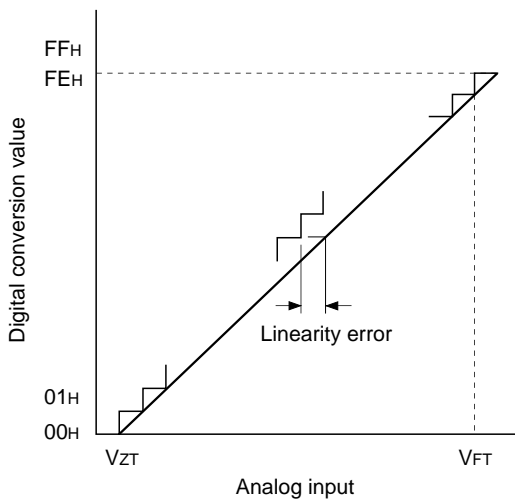
Fig. 4. Serial transfer CH0 timing



**(3) A/D converter characteristics** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, AVREF = 4.0 to AVDD, VSS = AVSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = 5.0V VSS = AVSS = 0V			±3	LSB
Zero transition voltage	VZT*1			-10	10	70	mV
Full-scale transition voltage	VFT*2			4930	4990	5050	mV
Conversion time	tCONV			160/fADC*3			µs
Sampling time	tSAMP			12/fADC*3			µs
Reference input voltage	VREF	AVREF		VDD - 0.5		VDD	V
Analog input voltage	VIAN	AN0 to AN7		0		AVREF	V
AVREF current	IREF	AVREF	Operation mode		0.6	1.0	mA
	IREFS		SLEEP mode STOP mode 32kHz operation mode			10	µA

**Fig. 5. Definition of A/D converter terms**



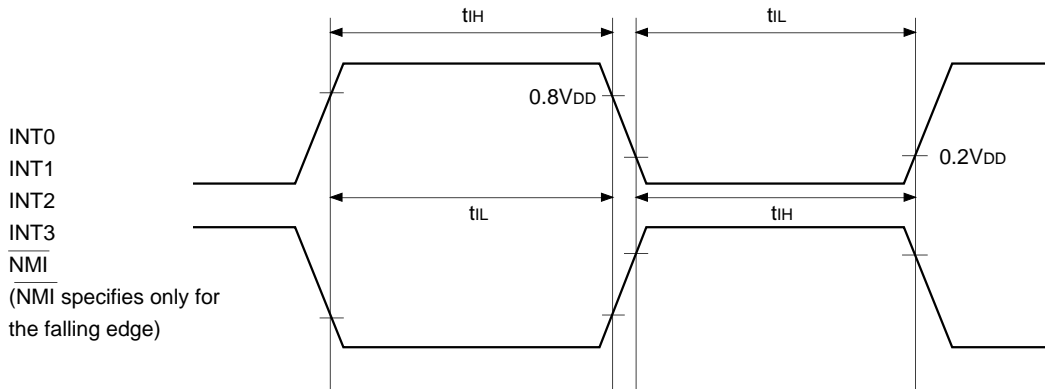
- \*1 VZT: Value at which the digital transfer value changes from 00H to 01H and vice versa.
- \*2 VFT: Value at which the digital transfer value changes from FEH to FFH and vice versa.
- \*3 fADC indicates the below values due to the bit 6 (CKS) of A/D control resistor (address : 00F9H) and the Bit 7 (PCK1) and Bit 6 (PCK0) of clock control resistor (address : 00FFH).

PCK1, 0	CKS	
	0 (φ/2 selection)	1 (φ/2 selection)
00 (φ = fEX/2)	fADC = fc/2	fADC = fc
01 (φ = fEX/4)	fADC = fc/4	fADC = fc/2
11 (φ = fEX/16)	fADC = fc/16	fADC = fc/8

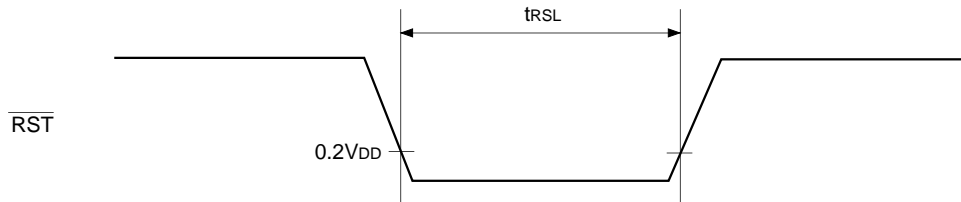
**(4) Interruption, reset input** (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t <sub>IH</sub> t <sub>IL</sub>	INT0 INT1 INT2 INT3 $\overline{\text{NMI}}$		1		μs
Reset input Low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/fc		μs

**Fig 6. Interruption input timing**

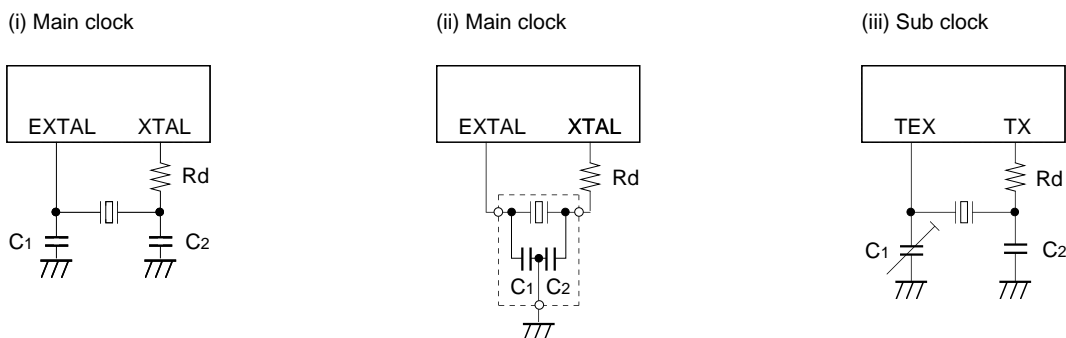


**Fig. 7.  $\overline{\text{RST}}$  input timing**



Appendix

Fig. 8. Recommended oscillation circuit



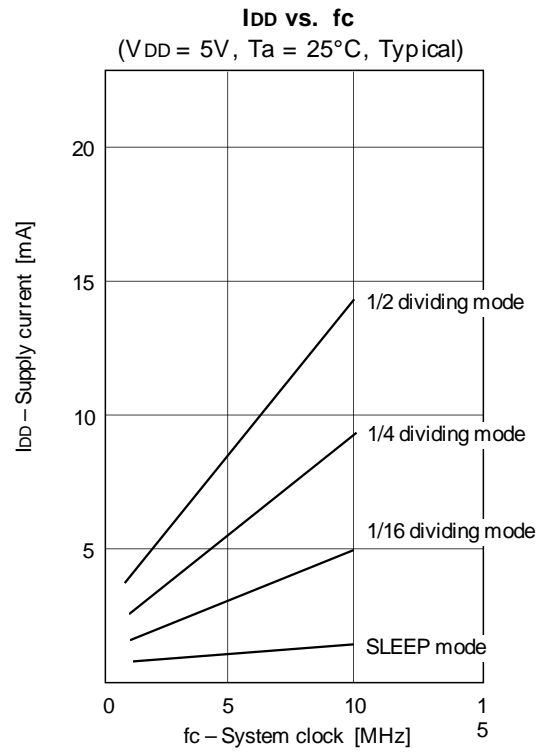
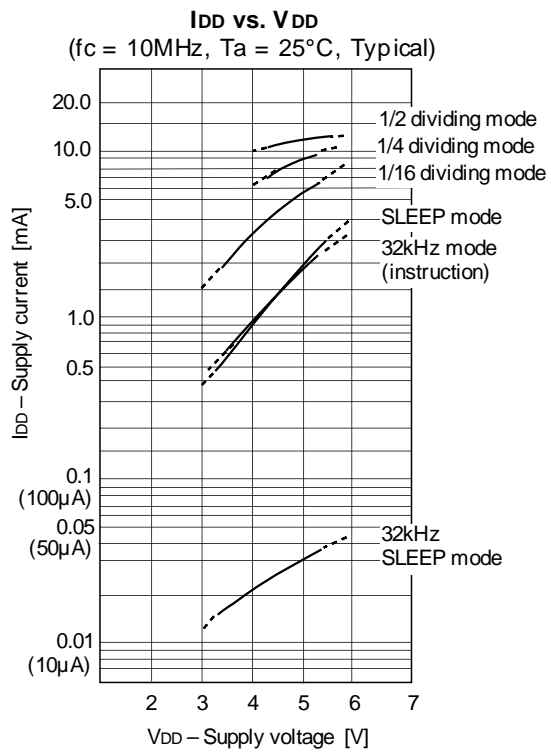
Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.00MTW*	10.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

Those marked with an asterisk (\*) signify types with built-in ground capacitance (C1, C2).

Selection Guide

Item	Mask product	CXP844P16Q-1-□□□
Package	80-pin plastic QFP	80-pin plastic QFP
ROM capacitance	12K bytes/16K bytes	PROM 16K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent

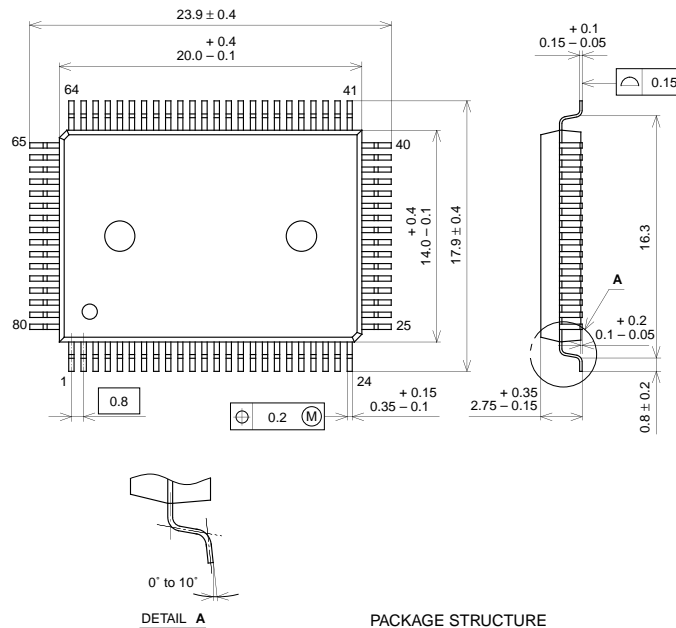
Characteristics curves



Package Outline

Unit: mm

80PIN QFP (PLASTIC)

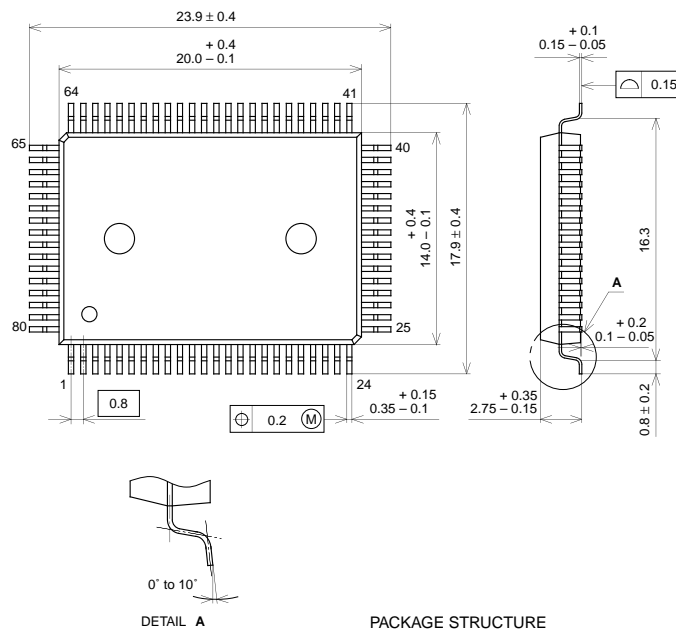


SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN QFP (PLASTIC)



SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm