Implementing 5-Million Gate Class Systems on a Single Chip

0.25-μm Generation System LSI Design Technology

- Enables the design of 5-million gate class LSIs
- Supports on-chip DRAM
- Verilog HDL/VHDL sign-off
- Automatic test generation (full scan and JTAG supports)
- Low power design

From the standpoint of manufacturing precision, the advanced system LSIs that support the latest AV and IT equipment are now entering the quarter micron (0.25 μm) era. From the standpoint of design methodology, a period that could be called the IP*1 era, as represented by the VSI*2 alliance, is about to commence; this will also be an era that sees increasing use of high level design such as RT*3 level and behavior level. From the application standpoint this will be an era characterized by digital processing of communications and image data in portable telephones, DVDs, and digital TVs, and by the increasing “personalization” of these applications.

To prepare for this era, Sony has completed its ASC6 design environment, which supports the implementation of 0.25-μm generation system LSIs, and is proceeding with preparations to begin shipment of these products. (See photograph 1.) As was the case with ASC5, which is the current generation (a 0.35-μm generation), we have prepared IP modules with general-purpose functionality, a wide range of interfaces, and analog functionality based around a core technology that supports on-chip DRAM, and also provide an easy-to-use design environment that incorporates the latest CAD technology to support our customers’ system LSI development. This article presents an outline of Sony’s 0.25-μm generation system LSI design technology.

*1: Intellectual property
*2: Virtual socket interface
*3: Register transfer

**Photograph 1  ASC6 Cross Section**

**Table 1  ASC6G/A, EGA Product Overview: C6MX-HS Series (2.5 V)**

<table>
<thead>
<tr>
<th>Product Overview</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VSS –0.5 to +3.5V</td>
</tr>
<tr>
<td>I/O voltages</td>
<td>VSS –0.3 to VDD +0.3V</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>–20 to +75°C</td>
</tr>
</tbody>
</table>

**<Absolute Maximum Ratings>**

| Supply voltage | 2.5V ± 5% |
| Delay time     | Internal gates: 35 ps *1/78 ps *2 |
| Power consumption | Internal gates: 0.07 μW/G/MHz *1 |
| Output drive capacity | Icc = 2, 4, 8, 12, 24mA |
| Interface levels | 2.5 V CMOS (JEDEC standard) |
| Process        |Four metal layer 0.25-μm silicon gate CMOS process |

*1: Inverters, fanout = 1
*2: Two-input NAND gates, fanout = 4 + standard interconnect load (200 μm)

**Product Overview**

Table 1 presents an overview of the ASC6 gate array (G/A) and embedded gate array (EGA) products. The ASC6 G/A and EGA products adopt a new cell structure to increase the integration density by about 30% as compared to earlier structural cells of the same generation, and to achieve integration densities approaching those of standard cells (S/C). This technology achieves a power consumption level of 0.07 μW/G/MHz*4. This level is about 20% lower than the earlier structural cells of the same generation, and less than
1/4*5 of that of the current generation (ASC5). The speed achieved by this new technology is about 1.8 times*5 that of the ASC5 product, namely, an internal gate delay time of 35 ps.*4

*4: Inverters; fanout = 1.
*5: As compared to the C5G-HS series at 3.3 V.

Function Macros

1. Function macros

The increased integration densities due to the advances in manufacturing technology allow most functions to be implemented as single-chip system LSIs in the few-million gate class. (See figure 1.) Thus the reuse of design assets and the distribution of “intellectual property” have become absolutely necessary for the development of large-scale LSIs in short periods. To support our customers’ system LSI development, Sony plans to supply as they become available Sony’s functional macros, including our analog macros as represented by our well-received A/D and D/A converters. These will include the following:

- A 32-bit RISC core
- An Sony-developed CISC core
- An image compression and expansion core
- Network and communication systems cores
- Protocol control cores
- Special I/O
- Analog cores

2. Parametric cells

Sony provides parametric cells. These cells, which include memory such as SRAM and ROM and functions such as multipliers, generate optimal functions by compilation to a specified size and structure optimal for the application. Table 2 lists the main products in this lineup.

ASIC DRAM
(Embedded DRAM)

Although there are signal-processing LSIs that form system cores, and memory ICs to store audio and video data in multimedia equipment that handles audio and video data, these functions are still implemented on separate chips. However, as systems get faster, structures based on individual chips can no longer provide the required data processing speed. That is, it is now necessary to incorporate the previously external mass memory into the signal-processing LSI itself. The merits of providing DRAM on chip in this matter are not merely a reduction in the number of parts and a reduction in the printed circuit board mounting area, but also include a significant increase in data transfer rates, i.e. bandwidth, and reductions in total system power consumption.

At Sony, we refer to on-chip DRAM in logic LSIs as “ASIC DRAM”. We first focussed on this technology in the ASC4 product (the 0.5-µm generation) and have developed and accumulated mass production experience with signal-processing LSIs for MD players in the ASC5 product. (See photograph 2.) In the ASC6 product we are developing ASIC DRAM in the class of up to 16 megabits per macro (see photograph 3) to respond to customer needs.

Table 2 Parametric Cell Products

<table>
<thead>
<tr>
<th>Type</th>
<th>Max. size</th>
<th>Organization (bits/words)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-port SRAM</td>
<td>Standard</td>
<td>40 kbits</td>
</tr>
<tr>
<td></td>
<td>High speed</td>
<td>72 kbits</td>
</tr>
<tr>
<td>2-port SRAM</td>
<td>Standard</td>
<td>40 kbits</td>
</tr>
<tr>
<td></td>
<td>High speed</td>
<td>72 kbits</td>
</tr>
<tr>
<td>ROM</td>
<td>Synchronous</td>
<td>256 kbits</td>
</tr>
<tr>
<td>Multiplier</td>
<td>4 x 4 to 1024 x 1024 (Parameterized macro)</td>
<td>16 x 16, 24 x 24, 32 x 32 (Fixed macros)</td>
</tr>
</tbody>
</table>
0.25-µm Generation System LSI Design Environment

1. High level design interface
Top down design using a hardware description language is indispensable in the design of large-scale system LSIs. At Sony, signoff is possible under a design environment using Verilog HDL or VHDL *6 as the hardware description language, using Verilog XL/VCS *7 or Model Sim/QuickHDL *8 as the logic simulator, and using Design Compiler*9 as the logic synthesis tool. (See figure 2.) Our customers can design Sony 0.25-µm generation system LSIs under this signoff environment.

2. Accurate simulation
Because of calculate the delay time while taking the input slew rate into account (see figure 3), the Sony logic simulator supports high-precision gate-level simulation. This design environment also includes a timing analyzer that analyzes static timing issues such as critical path timings and those associated with clock skew verification. We can support the MOTIVE*10 under the same environment. This design environment also supports accurate actual interconnect delay simulation, which is performed after layout design. Interconnect delay calculation uses parasitic interconnect resistances and capacitances extracted from the layout pattern. It also takes account of coupling capacitance. (See figure 4.)

*6: Sony supplies a VHDL library that conforms to the VITAL standard.
*7: Verilog-XL is a product of Cadence Design Systems, Inc. (USA). VCS is a product of Synopsys, Inc. (USA).
*8: Model Sim is a product of Model Technology (USA). QuickHDL is a product of Mentor Graphics Corporation (USA).
*9: Design Compiler is a product of Synopsys, Inc. (USA).
*10: MOTIVE is a product of Synopsys, Inc. (USA).
3. Design for test

Scan path technology generates test patterns automatically and frees customers from the need to create test patterns. This Sony-developed technology complements and enhances the gated clock technique, which is important for low-power design, and frees the customer from the need to add clock bypass routes. Since the scan-path routing is optimized during layout design, scan-path overhead is held to a minimum. (See figure 5.) Additionally, the BIST technology is used to test on-chip parametric ROM and RAM. This design environment also supports the JTAG standard (IEEE 1149.1) for board-level testing. All the scan-path, BIST, and JTAG circuits are inserted into the customer’s design automatically.

4. Low-power design technology

In the ASC6 product, Sony process technology has achieved a 75% reduction in power consumption from that of the ASC5 product. Additionally, Sony has begun to support Power Compiler, which optimizes the design circuits. Power Compiler reduces power consumption by up to 10% over the logic synthesis tool with almost no additional effort on the part of the user. Sony has also introduced gated clock tree synthesis (gated CTS). Clock gating methods reduce power dissipation by controlling the clocks input to each functional module. During synthesizing the clock tree, clock-skew adjustment is performed automatically, from the buffer output to each flip-flop in the following stage.

Future Developments

DVD, MD, digital TVs, and digital cameras are expected to become increasingly integrated with information processing equipment, and thus become truly easy-to-use products. Sony is aiming and striving for a true fusion of the audio/video and information technology worlds. The technology for integrating a total system on a single chip is becoming critically important in this transitional period. System LSI design technology centered around Sony’s on-chip DRAM technology will play that role, and Sony is committed to continuing to press forward in this area. In particular, Sony is now developing the 0.18-µm process technology generation, which will be the next generation after the 0.25-µm generation. At the same time, Sony will expand its product line of core circuits, such as CPU cores, and continue its efforts to make the design of system LSIs even easier.

*11: Built-in Self Test
*12: Joint Test Action Group
*13: Power Compiler is a product of Synopsys, Inc. (USA).