ACX399AKZ

Transmissive 2.9-Type nHD (640 × 360) Mobile Phone LCD Module Features Multi-Resolution Support IC, Wide Viewing Angle, and the VSPEC III™ High-Contrast LCD Mode

Higher resolution, wider viewing angles, and higher contrast are being demanded more strongly than ever for mobile phone displays. The newly-developed Sony ACX399AKZ is the first mobile phone display to adopt VSPEC III™, and achieves OLED levels of optical characteristics despite the high resolution of 253 ppi.
It also supports the FlatLink™ *1 3G interface and includes a driver IC that provides an automatic backlight brightness control function.

*1 FlatLink is a trademark of Texas Instruments Incorporated.

- New LCD mode (VSPEC III™) adopted
- Multi-resolution support IC
- Automatic backlight brightness control function IC
- Supports the FlatLink™ 3G interface

VSPEC

* "VSPEC" and VSPEC are trademarks of Sony Corporation.

New LCD Mode (VSPEC III™) Adopted

The ACX399AKZ adopts the VSPEC III™ wide viewing angle mode. This achieves OLED levels of optical characteristics despite the high resolution pixels. The contrast is 1000:1 and the device achieves a viewing angle of 160° in the up/down and/or right/left directions. The response time for intermediate levels is significantly improved, even compared to the existing VSPEC II™ wide viewing angle mode. (See table 2.)

Multi-Resolution Support IC

Sony developed and includes in the ACX399AKZ an IC that supports the following resolutions: nHD (640 × 360), HVGA (320 × 480), VGA (480 × 640/640 × 480), and WVGA (480 × 800/800 × 480). (See table 3.)
This is a highly compatible IC and will contribute to Sony's high-end LCD module products in the future.

Automatic Backlight Brightness Control Function IC

Sony has adopted this technology, which optimizes the backlight brightness and video signal together according to the displayed image and reduces current consumption without adversely affecting picture quality. (See figure 1.) This can contribute to longer battery life in mobile phones.

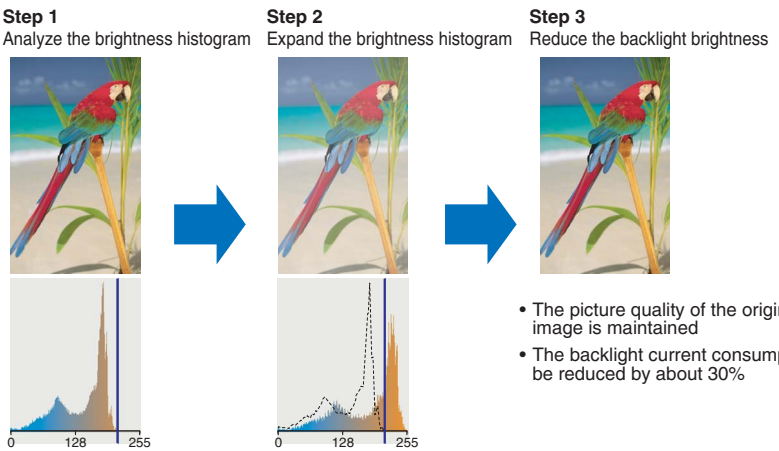
Supports the FlatLink™ 3G Interface (CDP)

The ACX399AKZ adopts the FlatLink™ 3G interface, which is a serial transmission technique using high-speed differential signals to support the transmission of the large volumes of data due to the ultrahigh resolution and multicolor display. (See table 1.) Sony also included EMI countermeasures designed using simulation and achieved low EMI characteristics.

V O I C E

We have developed an attractive LCD module product by combining the VSPEC III™ LCD mode for the first time in a mobile phone device and a highly general newly-developed LCD driver. The main feature of this module is that it achieves optical characteristics equivalent to those of organic EL displays. In addition to the optical characteristics, it features low power consumption and low EMI, and thus is a design that takes end product design into consideration. I strongly recommend that you consider using this module.

Figure 1 Automatic Backlight Brightness Adjustment Function IC



- The picture quality of the original image is maintained
- The backlight current consumption can be reduced by about 30%

Table 1 Main Specifications

Item	ACX399AKZ
Number of pixels	nHD (640 × 360 × RGB)
Diagonal size	2.9-type, landscape
Display mode	Transmissive, normally black
Interface	High-speed serial (FlatLink™ 3G)
Contrast	1000:1
Power consumption	23 mW (for all white display)

Table 2 VSPEC III™ Mode Features

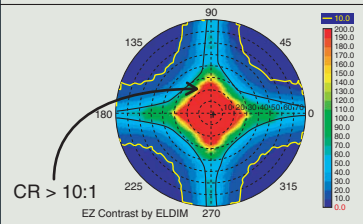
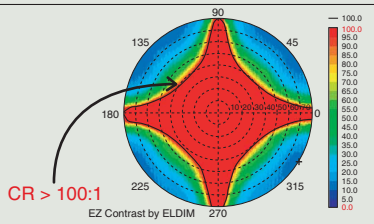
LCD mode		VSPEC II™	VSPEC III™
Viewing angle characteristics		 CR > 10:1	 CR > 100:1
Viewing angle		170°@CR > 10:1	170°@CR > 100:1
Response time	ON + OFF	20 ms	30 ms
	Worst	50 ms	40 ms

Table 3 LCD Driver Specifications

Item	LCD driver specifications
Supported resolutions	nHD (640 × 360) HVGA (320 × 480) VGA (480 × 640, 640 × 480) WVGA (480 × 800, 800 × 480)
Chip size	17.5 mm × 0.98 mm
Chip thickness	250 µm (with Polish)
Interface	High-speed serial (FlatLink™ 3G)
RAM	Partial RAM (864 × 160 × 3)
Added functions	Automatic backlight brightness control function
Supply voltage	V_{DDI} = 1.65 to 1.95 V V_{PNL} = 2.30 to 4.80 V
Process rules	CMOS 0.16 µm

Figure 2 Block Diagram