

High-Performance DVB-T COFDM Demodulator Featuring ZIF Interface and Best-in-Class Power Consumption

CXD1968R

Reducing system cost and improving reception performance are key drivers in the DVB-T COFDM demodulator system.

Sony has addressed both these issues with the introduction of the CXD1968R; Sony's 4th generation COFDM demodulator which will support future Zero IF tuners while meeting the stringent performance standards necessary for robust decoding under challenging reception conditions, such as Single Frequency Networks (SFN) and portable applications.

This excellent performance has been achieved with the added benefits of highly flexible configuration options and a class-leading low power consumption of only 150 mW.

- Meets all latest worldwide DTTV (Digital Terrestrial Television) specifications
- Zero IF interface (ZIF) for use with future silicon tuners
- Lowest power DVB-T demodulator on the market
- Flexible clocking options save cost by using tuner crystal clock source
- Auto acquisition/recovery controller minimizing host processor software overhead

■ Meets All Latest Worldwide DTTV Specifications

There are many different DTTV specifications worldwide which the receiver design had to address. One of the most challenging was the Scandinavian Nordig Unified specification which along with many others required development of new signal processing functions, such as handling signal echoes located outside the COFDM guard interval, or reducing losses in time-varying channels that might occur with an indoor aerial. Meeting these DTTV specifications gives Sony an essential competitive advantage.

■ Zero IF Interface (ZIF) for Use with Future Silicon Tuners

Sony is developing ZIF silicon tuner ICs to reduce cost and size of the DTTV front-end, as well as support mobile DTTV receiver applications. The CXD1968R is designed to operate with these new ZIF tuners (as well as existing IF tuners), by including extra signal processing functions to minimize unique ZIF tuner signal impairments, such as I/Q amplitude/phase imbalances, and DC offsets. Using a ZIF interface significantly reduces board area and component count for our customers.

■ Flexible Clocking Options Save Cost by Using Tuner Crystal Clock Source

Reducing system design cost is vital in a fiercely competitive DTTV receiver market. A significant cost saving was made by eliminating the separate demodulator crystal. An on-chip PLL driven by the tuner crystal oscillator generates the required clocks. Careful attention to signal integrity during IC design and layout was essential.

■ Auto Acquisition/Recovery Controller Minimizing Host Processor Software Overhead

Sony requested a reduction in the host processor software overhead during channel zapping and recovery. A hardware state-machine based controller was added to quickly acquire/re-acquire the DTTV signal whenever a new signal acquisition is needed without any host processor intervention. This feature reduces work and time to market for our customers.

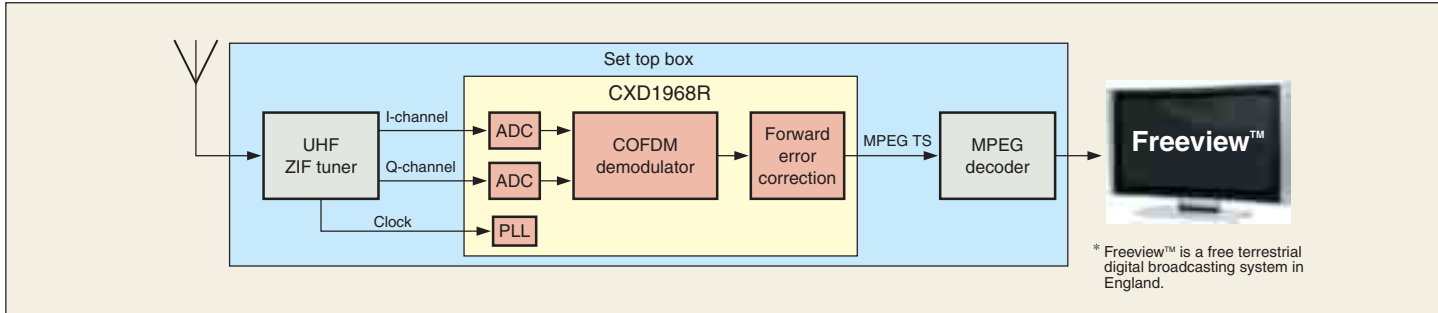
■ Lowest Power DVB-T Demodulator on the Market

Power consumption is a key feature in portable applications such as Memory Stick or USB TV receivers, but also in compact Set-Top-Box and IDTV (integrated DTV) designs, which must also remain in standby mode for long periods of time. The CXD1968R has class leading operating power consumption of 150 mW, as well as a very low standby power consumption.

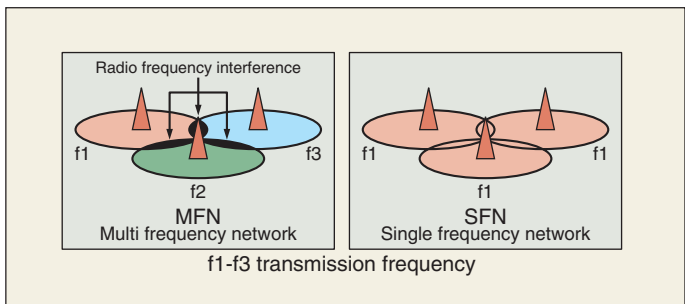
V O I C E

The major issue was keeping up with the fast pace of change of the DTTV receiver market and meeting the varied worldwide customer requirements. Many country specific specifications needed to be addressed in the design of the CXD1968R demodulator.

The design, development and mass production plan were modified and the subsequent design changes were undertaken efficiently and with a very high level of quality. The resulting ES worked first time and still met the original Sony customer schedule.



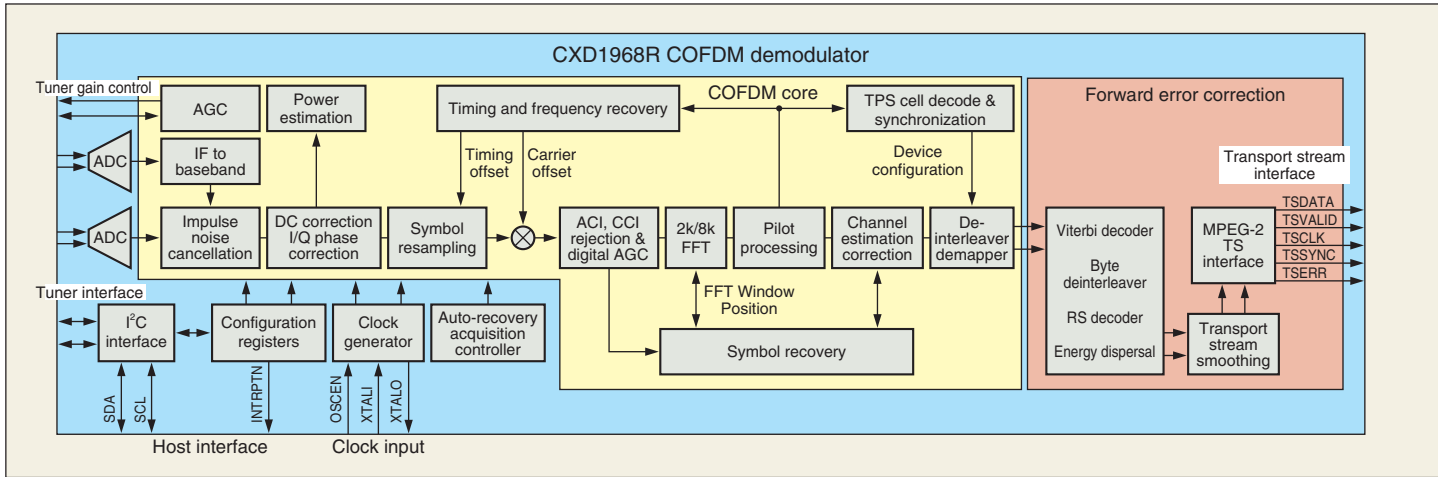
■ Figure 1 System Block Diagram



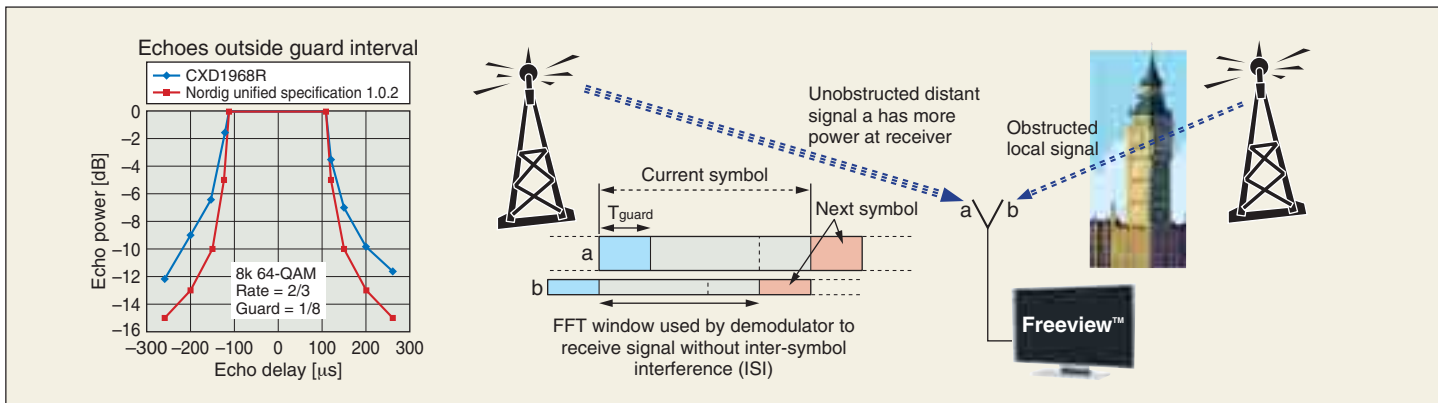
■ Figure 2 Single Frequency Networks (SFN vs. MFN)

■ Table 1 Main Specifications

Product name	CXD1968R
Power consumption	150 mW (IF), 185 mW (ZIF)
Supply voltage	3.3 V (Analogue/IO), 1.2 V (Core)
Clock frequency	4, 8, 16, 20.5 or 20.48 MHz
Operating temperature range	0 to 70°C
Package	64-pin LQFP



■ Figure 3 IC Block Diagram



■ Figure 4 Echoes Characteristics