FEATURING

Image Sensor Simulation Technology

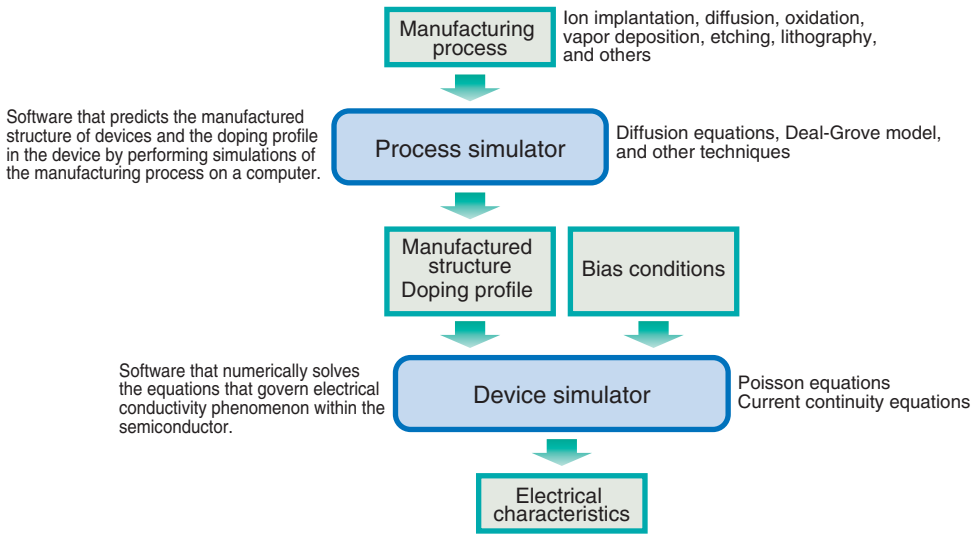
Unique Sony Design Technologies that Support Image Sensor Development

- 3D simulation
- Simulation accuracy
- GUI* that increases simulation efficiency
- Adopting the design of experiments method for increased efficiency

* GUI: Graphical User Interface

Image sensors make the number of applications such as camcorders, digital still cameras, and cellular phone, that includes itself greater. Pixel is scaled down year by year according to high resolution that make high-magnification digital zoom possible. Smaller pixel sizes, however, make it increasingly difficult to provide good device characteristics, such as sensitivity and saturation signal, and furthermore affect the other characteristics that were previously not thought to be influenced. Another issue here is that as the end product development cycle becomes shorter, the device development period is also becoming shorter every year. Thus given these conditions, the semiconductor simulator, which makes it possible to shorten development periods and reduce development costs, has become indispensable in contemporary semiconductor device development.

When Sony first began to develop image sensors, they developed independently their own dedicated image sensor process and device simulators in an effort to predict device characteristics and shorten the development period. In this article, we present an overview of Sony's process and device simulation technologies that support Sony's CCD development.

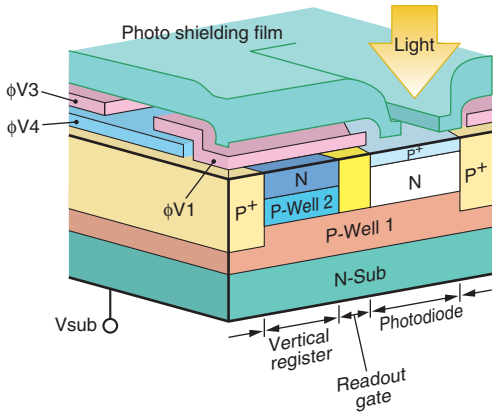


■ Figure 1 Process Simulator, Device Simulator

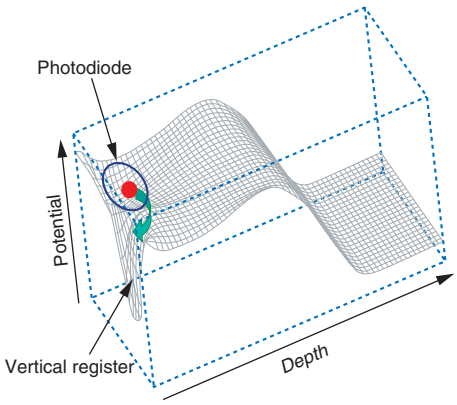
3D Simulation

The part of the image sensor structure that is its “eye”, i.e. the pixel, has a structure that differs from that of a MOS transistor in that it has a pattern that is asymmetric in both the left/right and up/down direction. As a result, the 2D simulation techniques used for MOS transistors cannot be used for image sensors. Therefore Sony, very early on, developed their own 3D simulator and have been using it in image sensor development ever since. This 3D simulator was developed to match the features of the CCD process and device structure, and, from the process aspect, adopts a physical model that takes into consideration diffusion during high-temperature oxidation and aims at speeding up the calculations concerning low-concentration ion implantation. From the device standpoint, this simulator adopts algorithms that can calculate the boundary conditions as periodic conditions, since the CCD pixel pattern is periodical.

To improve ease of use, this simulator was implemented so that it can accept simulations with multiple drive conditions (the same structure but different bias conditions) in a single input file. Using thus 3D simulator to predict device characteristics and determine prototyping conditions can contribute to shortening the prototyping period significantly and reducing development costs.



■ Figure 2 CCD Device Structure



■ Figure 3 Readout Simulation Potential

Simulation Accuracy

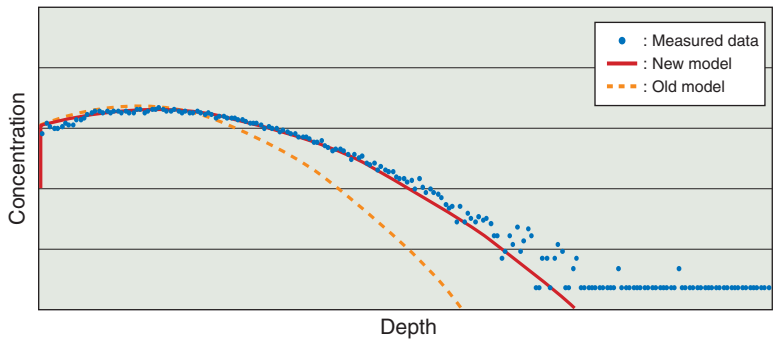
After accumulating charges from the photodiodes, a high voltage is applied to the readout electrode and the accumulated charges are read out to the vertical register in the CCD. Since a high voltage is applied to the electrode, a high insulation film breakdown voltage is required. Although the electrode insulation film was previously formed by a high-temperature oxidation process, it has become necessary to suppress the thermal diffusion of impurities in the silicon due to the scaling down the devices. Associated with this, Sony has switched to a simulator that has models capable of highly accurate prediction of the doping profile due to thermal diffusion. When using this new simulator, Sony has made a point of making the doping profile calculated by the simulator match the doping profile in the actual devices, and thus achieving even higher simulation accuracy.

Increasing Simulation Efficiency

No matter how good the accuracy of the simulator, if it isn't easy to use, it won't be able to withstand the demands of practical activities in the design process. Sony made a variety of improvements in operability and speed in the simulation design process flow. First, note that the simulation operation can be divided into the following three operations.

1. Creating the simulation input files
2. Running the calculation
3. Analyzing the results

Since the simulation input data is 3D, it is complex and difficult to create, and just coding this data is a time-intensive operation. Since it is a manual operation, coding mistakes can occur easily. To resolve these issues, Sony went to the effort of developing a GUI environment that creates the simulation data from mask patterns from the CAD layout tools and process condition tables. In this GUI environment, the designer creates the simulator input files by selecting the mask pattern and process conditions and setting up the simulation conditions. Thus the designer can perform all required operations through running the simulation even if the designer does not know the coding method used to create the simulation files. This makes it possible to perform in a few hours the work that previously required several weeks of hand labor. The simulator itself is implemented so that simulations are executed using optimized algorithms that take advantage of the features of the latest hardware and parallel processing. This results in simulation speeds 20 times faster than earlier systems. Although earlier simulators had limitations on the number of process steps due to simulator hardware restrictions, the upper limits have been improved greatly so that they are appropriate for today's hardware. Sony also developed a GUI so that the high volume of critical data produced by the simulator can be analyzed appropriately. Sony is developing a GUI for efficient statistical processing of data acquired from making a variety of changes to the process and device conditions. By graphing the changes in the device characteristics as the conditions change, designers will be able to immediately grasp the device characteristics.



■ **Figure 4 Simulation Accuracy**

Simulation Design Using the Design of Experiments Method

When using a simulator to determine prototype conditions, Sony simulators now perform simulations based on the DOE (Design of Experiment) improve efficiency even further. For example, with two levels and eight factors, it would be necessary to perform $2^8 = 256$ simulations. However, device characteristics can be predicted with just 16 simulations using the DOE. It is possible to quickly determine design conditions that will meet the specifications for multiple device characteristics by parallelizing the regression equations acquired by the analysis of a variety of characteristics. Also, the yield can be forecast by adding process variation to the parallelized equations. Sony has developed tools that perform the steps from analysis through determination of optimal conditions, and has significantly reduced the development time up to prototype creation.

Future Developments

The image sensor market is expected to continue to grow even faster in the future. Given these conditions, it is clear that the process and device simulation technologies presented here will become even more important in the future. Sony is aiming for even further improvements in accuracy and designer work efficiency, and is working on matching simulator results to actual devices and constructing even more efficient simulation environments. You can look forward to even more advanced image sensor process and device simulation technologies from Sony in the future.

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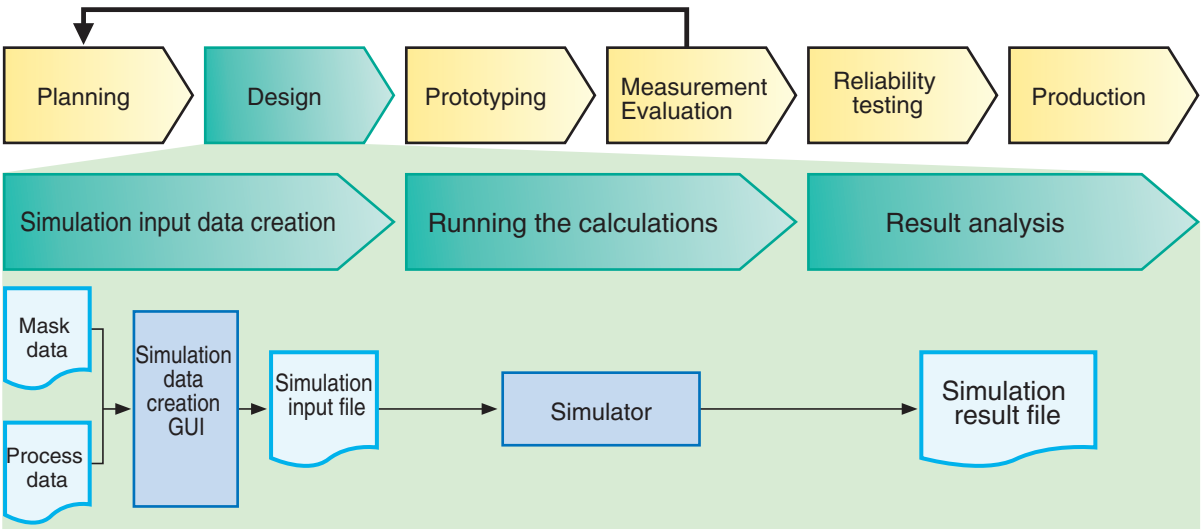

■ **Figure 5 Simulation Work Flow**