

# FEATURING

Low-Cost/Low-Power Electronic Toll Collection (ETC) Chipset Developed based on Unique Sony Technologies

## Second-Generation ETC Chipset

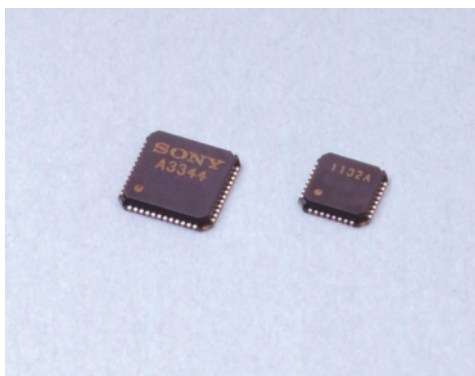
- A system that previously required a four-chip chipset is now implemented with just two chips
- Low cost
- Reduced mounting area
- The industry's top class of low-power performance

Japan's ETC (electronic toll collection system) is an automatic toll booth toll collection system for toll roads that does not require drivers to stop. The ETC unit in the car communicates wirelessly with a roadside antenna at 5.8 GHz and pays the required toll. Use of the ETC system reduces traffic jams at toll stations thus reducing the automotive exhaust and noise pollution associated with those traffic jams. Use of ETC for private cars started in 2001 and as of February 2005, the adoption ratio has exceeded 30%. Even more widespread adoption is expected in the future.

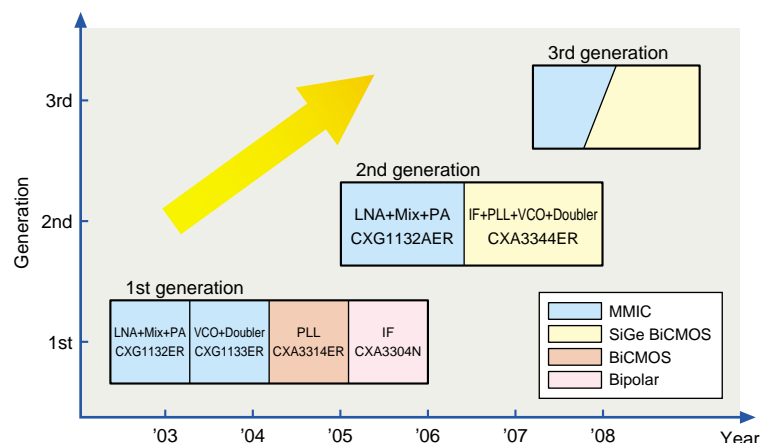
Sony has taken full advantage of the technologies it has developed over the years in the RF area to develop ETC chipsets from the very start of ETC system development and has earned a large share of the ETC in-car unit market.

The CXA3344ER and CXG1132AER presented in this article are products that were newly developed as a second-generation ETC chipset. By implementing in two chips a system that previously required four chips, these products can reduce both costs and mounting area in end products.

Another point is that as more and more electronic components have come to be used in cars, there is increasing demand for reduced power consumption in those components. While Sony's first generation chipset was a low-power system for its time, this second-generation chipset reduces current consumption by 26% during transmission and by 42% during reception, thus achieving the industry's top class of low power performance.



■ Photograph 1 Two-Chip ETC Chipset (CXA3344ER / CXG1132AER)



■ Figure 1 Development Trends in ETC Chipsets

## ETC Chipset Overview

### ETC system overview

The ETC system is allocated to the 5.8 GHz band and uses transmission (ETC in-car unit → ETC gate) and reception (ETC gate → ETC in-car unit) frequencies that are separated by 40 MHz. During transmission, after the local oscillator signal generated by PLL, VCO, and doubler circuits is modulated by an ASK modulator, that signal is amplified by a power amplifier to drive the antenna. During reception, after the signal input from the antenna is amplified by a low-noise amplifier, it is downconverted to 40 MHz using a local oscillator signal. This signal is ASK demodulated in the IF block.

Since these devices handle the high frequency of 5.8 GHz, most of the blocks that operated in that frequency band were fabricated in a GaAs process.

### ETC chipset structure

One major feature of this newly-developed ETC chipset is that unlike the four chips required for the previous chipset, this chipset only requires two.

Figure 2 shows the structures of both the earlier four-chip chipset and the newly-developed two-chip chipset. While in the earlier chipset the IF (RSSI, limiter, and peak hold) is implemented in the CXA3304N, the PLL is implemented in the CXA3314ER, and the VCO and doubler are implemented in the CXG1133ER, in the new chipset, the CXA3344ER integrates the functions of all three of these devices. At the same time, the CXG1132AER was developed as a low-power version of the CXG1132ER. Thus the CXA3344ER and the CXG1132AER implement a complete ETC chipset with just two chips.

### Reduced mounting area

Switching from a four-chip structure to two-chip structure reduced the mounting area by 27%. (See figure 3.)

Also, reducing the number of chips means that the cost of the chipset as a whole can be held to a minimum.

\*: The mounting area is calculated as the sum of the areas of the chip packages.

### Lower power

To reduce power consumption in the CXA3344ER and the CXG1132AER, Sony used their unique technologies to reduce the power in each semiconductor device circuit. As a result, this chipset reduces current consumption by 26% during transmission and by 42% during reception, thus achieving the industry's top class of low power performance. (See figure 3.)

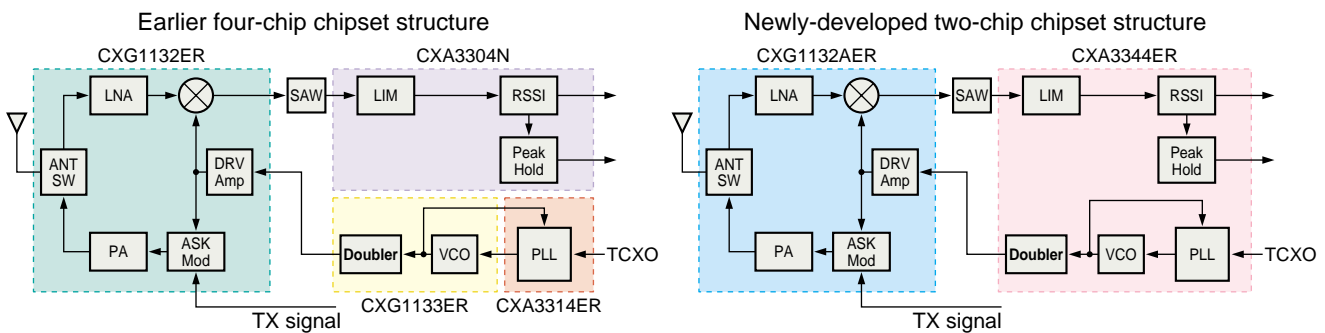


Figure 2 ETC Chipset Structures

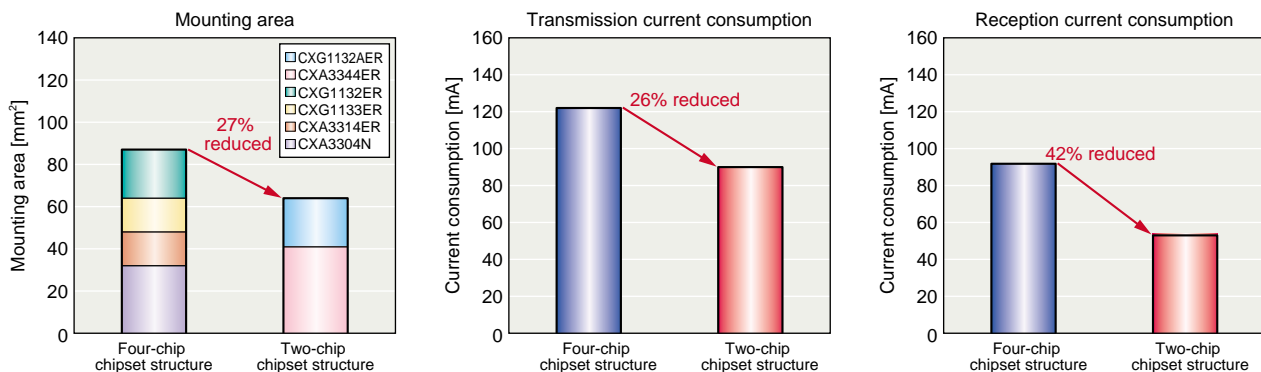


Figure 3 ETC Chipset Mounting Area and Current Consumption Comparisons

## IF/PLL/VCO/Doubler (CXA3344ER)

### Functions of three chips integrated on one chip

The CXA3344ER is fabricated in the latest SiGe BiCMOS process. The key to implementing IF, PLL, VCO, and doubler functions on a single chip was in discovering how to implement the VCO and doubler, which were previously implemented using a GaAs process, in the SiGe BiCMOS process.

In this IC, we made the 5.8 GHz block as simple as possible, and designed the circuits to take maximum advantage of the capabilities of SiGe BiCMOS devices.

### Reduced power consumption

The VCO and the doubler are the blocks with the largest current consumption. A new method was adopted for these blocks and their circuits were optimized relative to the other blocks, resulting in a total reduction in power consumption for the IC as a whole.

Figure 4 shows the structures of the VCO and doubler. In the earlier method, after a 2.9 GHz signal was generated by the VCO, that signal was amplified by a buffer amplifier. In the doubler, the secondary harmonic (5.8 GHz) of the 2.9 GHz signal was generated by amplifying and distorting the 2.9 GHz signal. After that, the 5.8 GHz signal was output by removing the 2.9 GHz component with a band elimination filter (BEF). This method, however, involves a complex sequence of circuits up to the point the 5.8 GHz is output and requires power proportional to that complexity.

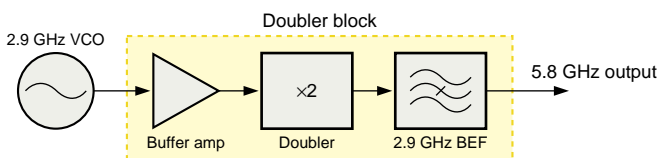
To resolve this problem, Sony developed a new circuit that directly converts the 2.9 GHz differential signal generated by the VCO to 5.8 GHz. This new system results in a 43% reduction of the total current consumption of the VCO and doubler compared to the earlier method.

### Automatic output level adjustment circuit

Since the 5.8 GHz output signal level is used by the CXG1132AER as the local oscillator signal, it is desirable that there be minimal changes in the output level with manufacturing variations and temperature fluctuations. To reduce these sorts of output variations, the CXA3344ER includes an automatic output level adjustment circuit.

In this method, the output level is automatically adjusted using the fact that the doubler drive current and the output level are correlated. Actually, a dummy circuit (doubler dummy) is used and the VCO is controlled so that drive current is the same as the reference value to monitor the doubler core drive current. This makes it possible to hold the output level precision to within  $\pm 2.5$  dB regardless of manufacturing variations or temperature changes. Additionally, the circuit is designed so that the output level setting can be adjusted with an external resistor ( $R_{ext}$ ). (See figure 5.) This makes it possible to adjust the output level to a value optimal for the customer's application.

Earlier VCO and doubler structure



Newly-developed VCO and doubler structure

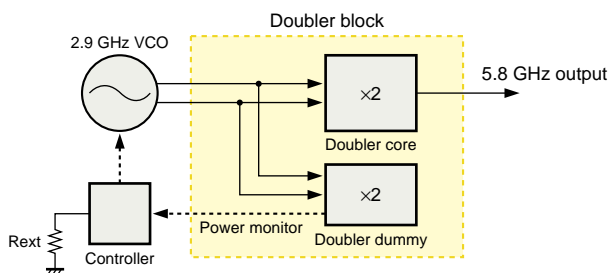


Figure 4 VCO and Doubler Structures

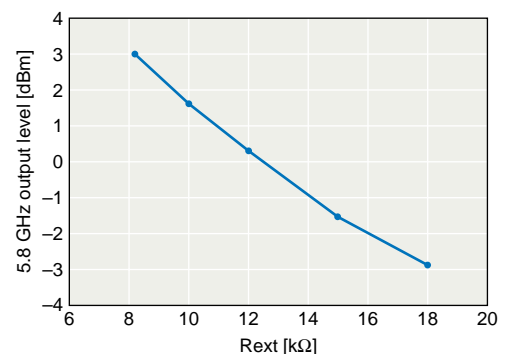


Figure 5 Output Level Characteristics

## LNA/Mixer/Power Amplifier (CXG1132AER)

### Development of an RF transceiver IC for ETC

Sony entered the market for cellular phone RF front end MMICs in the early 1990s. Since then Sony has continued to lead the industry by developing large numbers of MMIC\* devices (including antenna switches, low-noise amplifiers/mixers, and power amplifiers) using GaAs process technologies.

This ETC RF transceiver IC was designed and tuned based on technologies developed during the development of cellular phone MMICs, and is the largest scale MMIC Sony has yet attempted. By adopting the junction-gate FET process, which provides superlative sensitivity, distortion, and manufacturing stability characteristics, Sony achieved both high performance and low cost.

\*: MMIC: Microwave Monolithic Integrated Circuit

### From the CXG1132ER to the CXG1132AER

In developing the CXG1132AER of this release, Sony focused on two issues: reducing current consumption compared to the earlier product (CXG1132ER) and incorporating the externally applied bias circuit on the same chip.

To reduce current consumption, Sony reduced current consumption during reception in the driver amplifier for the local oscillator by optimizing the level diagram. Additionally, Sony increased the amplification efficiency of the local oscillator driver amplifier during transmission by reevaluating the power supply. These reevaluations of the circuits resulted in 43% and 17% reductions in current consumption during reception and transmission, respectively.

To incorporate the externally applied bias on the chip itself, Sony modified the circuits so that the power amplifier bias was not needed, thus improving the IC's ease of use.

### Future Developments

Japan's Ministry of Land, Infrastructure and Transport is studying a wide range of ITS\* services that take advantage of ETC communication technologies. These include automatic toll payment and non-stop in and out at for-fee parking facilities and providing information to in-car navigation systems at highway rest stops. At the same time, Sony is proceeding with the development of future generation ETC chipsets that will take advantage of the technologies nurtured in ETC chipset development up to now to provide further miniaturization, even lower power operation, and lower costs.

Keep your eye on Sony for the latest in high-frequency and process technologies.

\*: ITS: Intelligent Transport Systems

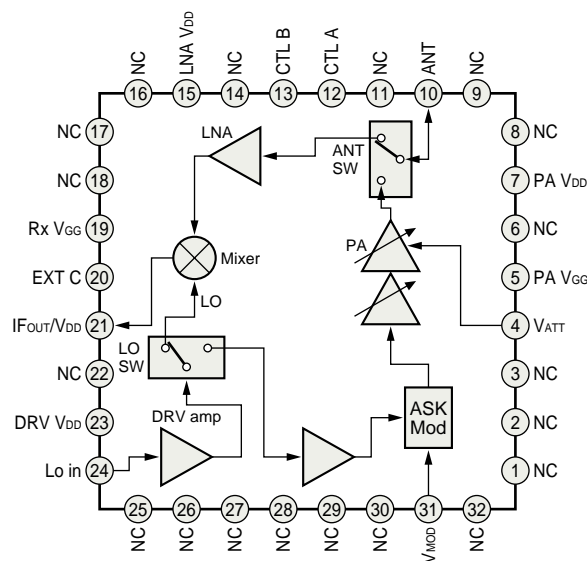


Figure 6 CXG1132AER Block Diagram