

Leading Edge Semiconductor Cleaning Technologies

Leading Edge Semiconductor Wafer Surface Cleaning Technologies that Support the Next Generation of Semiconductor Devices

- The industry's most advanced cleaning processes
- Technologies that support 45 nm and beyond CMOS devices
- Cleaning that does not collapse patterns
- Local area cleaning
- Fine particle detection technologies

In the manufacturing of key semiconductor devices, it is extremely important to reduce, as much as possible, the particle, metallic, organic, and other contamination (see table 1) that occurs in the manufacturing process and that causes rejects and degradation of device quality and reliability. Silicon substrate (wafer) cleaning has become a critical process that influences product yield, and processes that clean the wafers to assure yields make up 30 to 40% of the steps in the total manufacturing process. It is only these cleaning processes that can remove the particle and other contamination that occurs in semiconductor device manufacturing. (See figure 1.) Sony is working on developing new cleaning technologies for the manufacture of next-generation semiconductor devices, since advances such as finer fabrication, higher integration densities, and higher speeds are expected to continue at ever increasing rates. This article presents an overview of the next generation of semiconductor cleaning technologies.

Issues in Next-Generation Semiconductor Cleaning Technologies

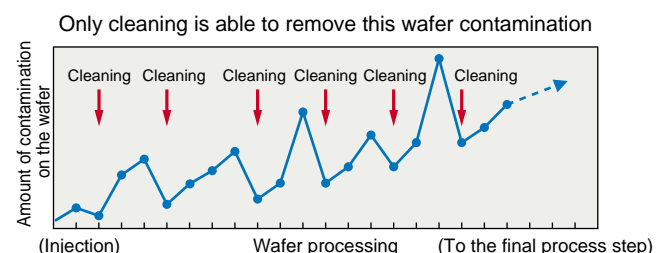
Even higher performance, higher functionality, and lower power will be required in the semiconductor system on chip (SoC) devices in future network and digital appliances. To achieve these requirements, circuit patterns will become even finer, from 90 nm to 65 nm and even 45 nm, and the number of interconnect layers will increase as well.

Furthermore, three-dimensional spatial structures, such as MEMS, have also appeared. The manufacturing processes required to fabricate these devices have become more complex, the number of process steps has increased, and the cleaning processes have changed radically as well due to finer device fabrication technologies, increasing device complexity, increasing numbers of interconnect layers, and the introduction of new materials.

In conventional semiconductor manufacturing lines, a wafer cleaning method called RCA cleaning that uses large-scale multi-tank immersion cleaning units has been used for many years now. (See figure 2.) In this technique, 25 to 50 wafers

■ Table 1 Wafer Contamination and Its Effects

Type of contamination		Main influences on device characteristics	
Particle contamination		Pattern defects Ion implantation defects Insulating film breakdown defects	
Metallic contamination	Alkali metals	MOS transistor instability Gate oxide film breakdown degradation	
	Heavy metals	Increased PN junction reverse leakage current Gate oxide film breakdown defects Minority carrier lifetime degradation Oxide excitation layer defect generation	
Chemical contamination	Organic contamination		Gate oxide film breakdown defects CVD film variations (incubation) Thermal oxide film thickness variations (accelerated oxidation) Haze occurrence (wafer, lens, mirror, mask, reticle)
	Inorganic contamination	Dopants (e.g. B, P)	MOS transistor Vth shifts Si substrate and high-resistance Poly-Si sheet resistance variations
		Bases (e.g. amines, ammonia)	Degradation of the resolution of the chemically amplified resist
		Acids (e.g. SOx)	Occurrence of particle contamination and haze due to the generation of salts
Natural and chemical oxide films (e.g. moisture, oxygen)		Increased contact resistance Gate oxide film breakdown degradation	



■ Figure 1 Importance of Cleaning in Semiconductor Device Manufacturing

are immersed in ammonium hydroxide + hydrogen peroxide + water, hydrochloric acid + hydrogen peroxide + water, and dilute hydrofluoric acid heated to 60 to 80°C for about 10 minutes each to remove particles, metallic contamination, and organic contamination from the wafer surface. After each chemical processing step, the wafers are rinsed in pure water for 10 minutes. This procedure produces a clean wafer surface. Since this process uses large amounts of chemicals and pure water, ways to reduce the amounts of chemicals and pure water used are desired to reduce both the costs of the chemicals and the burden on the environment. To resolve these issues, Sony developed a new wafer cleaning method, called SCROD*. (See figure 3.) This cleaning method sprays the wafer alternately for 5 to 10 seconds each with ozonated water and dilute hydrofluoric acid. Repeating this cycle a few times removes particles, metallic contamination, and organic contamination from the wafer surface extremely efficiently. This technique reduces the number of chemicals used to a single chemical, and reduces the volumes of chemicals and water used to 1/40 and 1/25 of their previous levels, respectively. This technology is used both for the PlayStation 2 CMOS chips manu-

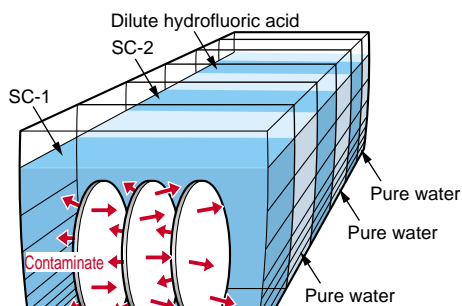
factured at the Fab1 and Fab2 lines at Sony Computer Entertainment (Nagasaki) and for the LCD and CCD video devices manufactured at the Sony Semiconductor Kyushu Corporation Kumamoto Technology Center. However, for semiconductor devices at the 45 nm circuit pattern size and beyond, there are major obstacles that even this SCROD technique cannot resolve. Since SCROD cleaning and other conventional cleaning methods all are wet cleaning techniques in which water and cleaning liquids are used, they are all subject to the problem that the surface tension of these liquids can collapse or destroy the fine device patterns. (See figure 4.) Although the circuit pattern size in earlier semiconductor devices was large enough to avoid being destroyed by surface tension, this problem has arisen due to the ultrafine patterns used in the 45 nm and beyond generations. Furthermore, there are also other issues, for example, it is harder for fluids to get into these fine structures and contamination may readhere since the cleaning operation is applied to the whole wafer. Another issue is that when developing cleaning technologies, it is necessary to detect to what extent contamination has been removed. The size of particles that adversely effect semicon-

ductor device yields and quality is about 1/2 that of the circuit pattern size. Thus as the size of the circuit patterns becomes smaller, it becomes necessary to detect how efficiently particles are removed by the cleaning process for particles down to the extremely small size of 30 nm and smaller. This article introduces and presents overviews of several new cleaning and detection technologies that are now under development at Sony as candidate technologies for resolving these issues and problems.

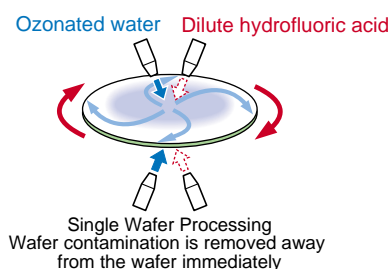
*: SCROD: Single-Wafer Spin Cleaning with Repeated Use of Ozonated Water and Dilute HF

Supercritical Fluid-based Cleaning Technology

Sony recognized that since supercritical fluids have zero surface tension, they represent a possible solution for the problem that surface tension of ordinary liquids can collapse the fine patterns on semiconductor devices, and is working on ways to apply these materials in the semiconductor cleaning process. Substances transform into any of the solid, liquid, and gas phases. However, if the



Batch processing of 25 to 50 wafers
Wafer contamination accumulates and recontaminates the wafers.



Single Wafer Processing
Wafer contamination is removed away from the wafer immediately

■ Figure 3 SCROD: Single-Wafer Spin Cleaning with Repeated Use of Ozonated Water and Dilute HF



CMOS LSI

When cleaned using liquids...

The surface tension of liquids can collapse the patterns in ultrafine device structures.

■ Figure 4 Issues for the Next-Generation Cleaning Process

temperature and pressure are increased above a critical point, they become a supercritical fluid, which combines characteristics of both the gas and liquid phase. For example, carbon dioxide becomes a supercritical fluid above 31 degrees Celsius and 7.3 megapascals. Supercritical fluids have the property that it has zero surface tension.

When a tiny amount of a cleaning agent is added to this supercritical fluid carbon dioxide and that is used to clean fine patterns, particle contamination is removed completely with no collapse whatsoever to fine patterns that would have been collapsed by conventional wet cleaning. (See figure 5.)

Note that in addition to semiconductor device manufacturing, this supercritical fluid-based technology can also be applied in areas such as electronic component manufacturing, nanotechnology, and biotechnology. The carbon dioxide used here is recovered and purified from the carbon dioxide generated when crude oil is extracted from oil fields, during oil refining, by thermal power plants, and by steel manufacturing. Furthermore, the carbon dioxide used in this cleaning tech-

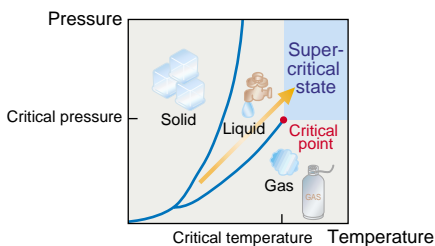
nology is recycled and reused, and thus does not lead to global warming. Additionally, this is an extremely environmentally friendly technology in that it uses no water whatsoever.

Cryogenic Aerosol-based Cleaning Technology

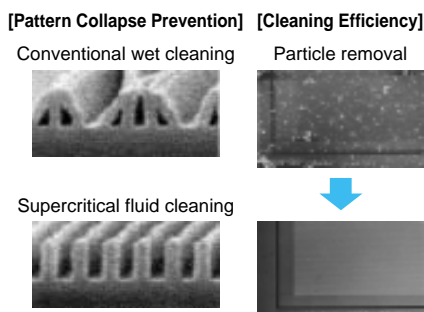
Cryogenic aerosol-based cleaning technology is another candidate technology under development at Sony that may be able to resolve the problem of collapse to fine patterns during cleaning. In this technique, the physical force of aerosols (gaseous suspensions of ultramicroscopic particles) sprayed at the fine patterns is used to clean the wafer. Since liquids are not used in this cleaning technology, no surface tension occurs. While there are existing cleaning methods that use carbon dioxide or argon aerosols, these aerosols do cause collapse to semiconductor patterns. However, by using nitrogen aerosols, which are lighter than these earlier aerosols, Sony discovered that wafers can be cleaned without collapse to the pattern. (See figure 6.)

Vapor Cleaning Technology

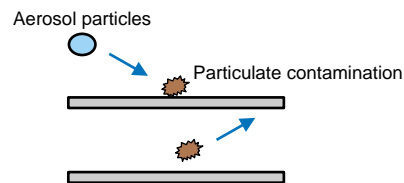
Sony is now developing vapor cleaning technology using chemical vapors as a cleaning technology that can clean even to the bottom of microscopic holes without collapsing fine patterns on a semiconductor wafer. Although there are already hydrofluoric acid vapor cleaning methods that work at room temperature and pressure, these techniques create residues and require a rinse with water after processing. When the wafer is rinsed, the surface tension collapses the fine patterns on the wafer. To avoid this problem Sony developed a technique in which the wafers are heated in a low-pressure chamber and cleaned with hydrofluoric acid vapor. This reduced pressure heating vapor technique does not generate residues, and thus does not require the post-processing rinse.



Material Phase Equilibrium Diagram



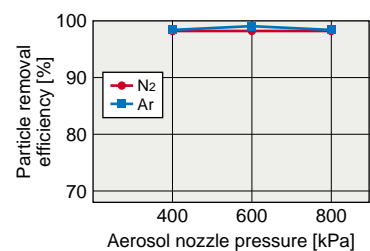
■ Figure 5 Supercritical Fluid-based Cleaning



[Pattern Collapse Prevention]



[Cleaning Efficiency]



■ Figure 6 Aerosol-based Cleaning

Local Area Cleaning Technology

While methods such as the ones described above all clean the whole surface of the wafer in a single operation, we think that as the required level of cleanliness gets even higher than it is now, local area cleaning, in which contaminating particles are targeted one by one, will become necessary. Sony is now engaged in speculative research on future cleaning technologies that are still only dreams. These include laser cleaning (see figure 7), in which particles are removed by being targeted with a laser beam and nanoprobe cleaning (see figure 8) in which a microscopic needle (nanoprobe) with a size measured in nanometers (10^{-9} meters) is used to remove particles by moving them physically.

Fine Particle Detection Technologies

To remove the extremely fine contamination such as that discussed above, it is first necessary to detect the contamination on the surface of the wafer and grasp the nature of the problem. For semiconductor devices with circuit pattern sizes of 45 nm

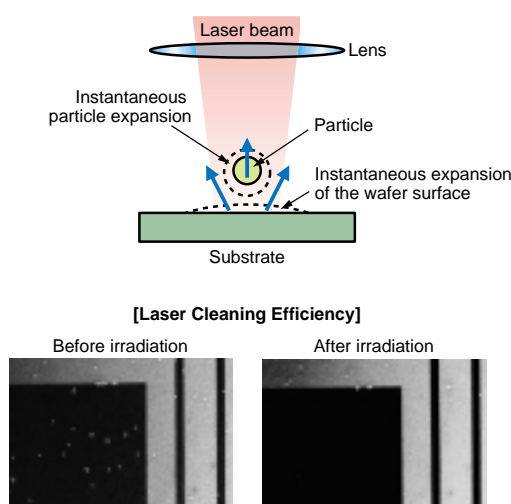
and beyond, submicroscopic particles with sizes of 30 nm and smaller can adversely affect yields and quality. The conventional method for detecting particles on the surfaces of wafers is laser scattering detection: the surface of the wafer is irradiated with a laser beam and the light scattered by the particles is detected. It is known that even smaller particles can be detected with this technique by using a laser beam with a shorter wavelength. Although wafer surface particle detection equipment that can detect particles in the 50 to 60 nm range using a 488 nm wavelength laser beam is commercially available, Sony is now developing technologies that can detect 30 nm and smaller particles using a Sony developed 266 nm deep-ultraviolet solid state laser.

It has now become necessary to detect particles on the surfaces of wafers used for SOI (Silicon on Insulator) devices, a technology that is expected to be adopted for manufacturing future high-performance low-power SoC devices. However, with the conventional detection technologies that use a 488 nm laser beam, the laser beam penetrates into the top silicon layer of the SOI wafer and is reflected from the insulating film inter-

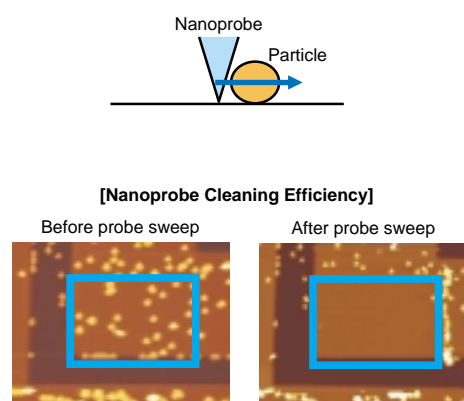
faces. These reflections interfere with the light scattered by the particles on the surface and the random reflections from unevennesses in the film interfaces generates detection noise, making particle detection difficult. However, since the short wavelength 266 nm laser beams used in this new detection technology does not penetrate into the top silicon layer of the SOI wafer, it is possible to measure just the light scattered by particles on the wafer surface. As a result, this system can detect surface particles with high precision. (See figure 9.)

Future Developments

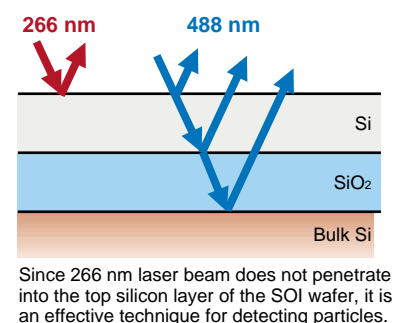
Sony is now engaged in research on detailed analysis of cleaning processes, explication of cleaning mechanisms, and the development of new cleaning equipment technologies with the goal of practical application of the new semiconductor cleaning technologies introduced here in Sony's next-generation semiconductor device manufacturing, such as 45 nm and beyond leading-edge CMOS device manufacturing. Keep your eye on Sony for the most advanced industry leading cleaning technologies.



■ Figure 7 Laser Cleaning



■ Figure 8 Nanoprobe Cleaning



Since 266 nm laser beam does not penetrate into the top silicon layer of the SOI wafer, it is an effective technique for detecting particles.

■ Figure 9 Fine Particle Detection Technologies