

FEATURING

Multilevel Wiring Technology for Leading-Edge CMOS Devices in the 65 nm Generation

Hybrid Low Dielectric Constant Film Structure Copper Wiring Module Reduced Wiring Capacitance and Supports Fine Fabrication

- Supports 100 nm half-pitch design rules
- Wiring that performs at the industry's highest level
- Hybrid low dielectric constant film structure
- Dual damascene copper wiring technology

In 2002, Sony started a joint development project with Toshiba to develop 65 nm generation ultrahigh speed embedded DRAM logic technologies. Sony has also already announced plant and equipment investment plans aimed at creating the industry's fastest mass production facility for the 65 nm generation using 300 mm wafers.

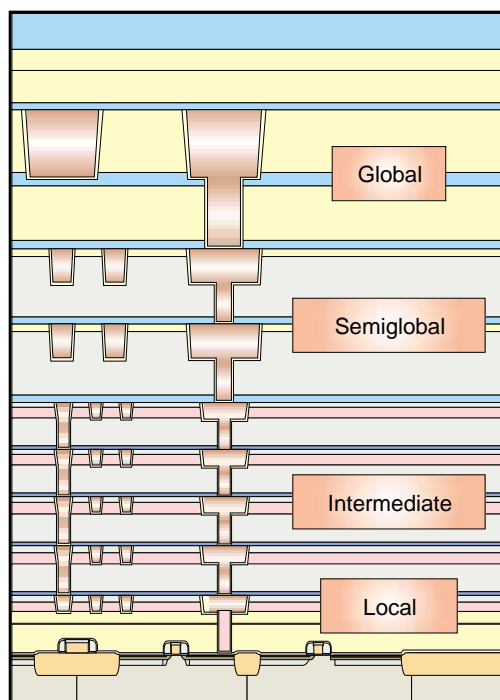
Figure 1 shows the expected cross section of a typical 65 nm generation CMOS device and table 1 lists the design rules for the wiring layers. Approximately 90% of the vertical structure, and approximately half the steps in the wafer process consist of the multilevel wiring processes that connect DRAM and transistors, and the influence of wiring characteristics on the whole device increases at each generation. As a result, even higher performance is required of the multilevel

wiring processes in the 65 nm generation than in the previous generation.

The wiring resistance and interlayer capacitance are important factors that limit the high-speed performance and ability to minimize power consumption in CMOS devices. Thus how low resistance and low capacitance the multilevel wiring process can be made without adversely impacting yield and reliability is a critical issue.

To respond to these requirements, Sony has now developed a hybrid dual damascene structure copper wiring module* as a unique Sony multilevel wiring technology.

* Copper wiring module: The whole multilevel wiring formation process that is completed by the combination of several elemental processes including insulation film formation, trench formation, and metal embedding.



■ Figure 1 Expected Cross Section of a 65 nm Generation CMOS Device

■ Table 1 65 nm Generation Multilevel Wiring Design Rules

Wiring layer	Pitch (nm)	Contact holes (nm)
Local	180 (240)	φ90 (120)
Intermediate	200 (280)	φ100 (140)
Semiglobal	400 (560)	φ200 (280)
Global	2000 (2000)	φ600 (600)

Note: Values in parentheses apply to the 90 nm generation.

Hybrid Dual Damascene

Hybrid dual damascene is a process for conductor formation that simultaneously forms wiring and contact holes (via) on an interlayer insulation film formed from a layer structure of low dielectric constant films with differing characteristics. Figure 2 shows a cross section of the hybrid dual damascene device structure. Its major features are that it adopts a layered low dielectric constant film structure that uses an organic film called polyarylether (PAE) as the interconnect insulation film and a carbon-doped silicon oxide (SiOC) inorganic insulating film as the interlayer film in which the contact holes are formed, and that it forms the embedded wiring using copper, which has a lower resistance than aluminum, as its main material. Sony focused on this hybrid dual damascene structure as a

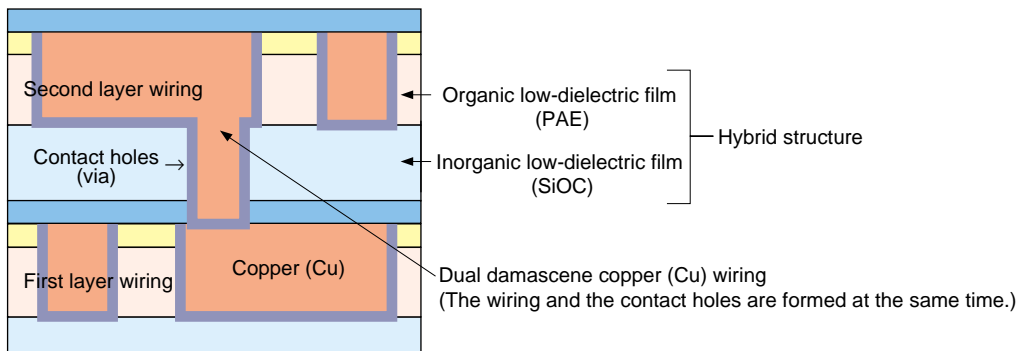
process that holds hope for improvements in both shape control characteristics and sample-to-sample variations in device characteristics as compared to the previous generation.

Target Wiring Performance and Low Dielectric Constant Film Structure

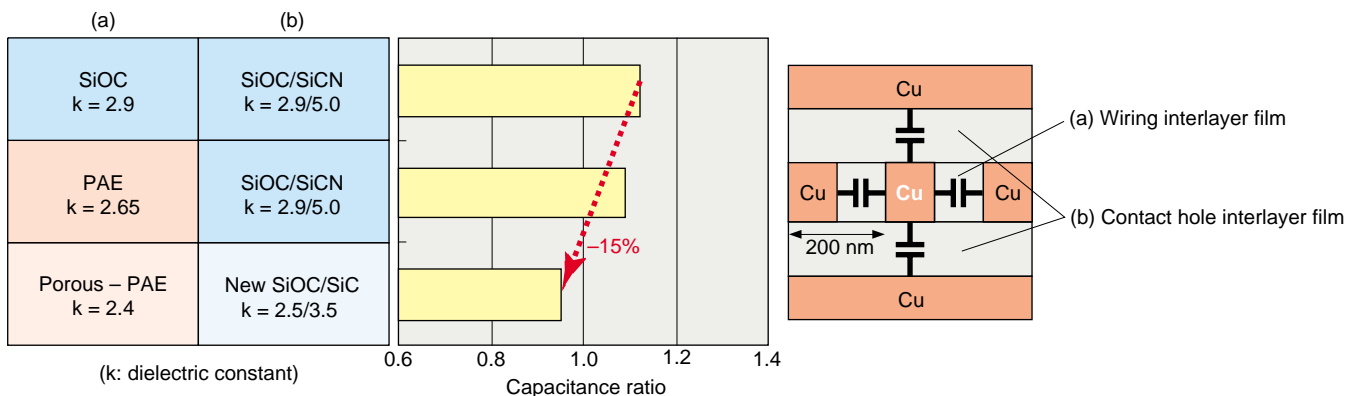
Figure 3 shows the result of simulating the wiring capacitance for various low dielectric constant film structures. A capacitance increase of approximately 12% due to the reduced interconnect spacing (140 to 100 nm) is expected if the carbon-doped silicon oxide/nitrogen-doped silicon carbide (SiOC/SiCN) film structure used in the wiring process in the previous generation are applied in the finer wiring fabrication of the 65 nm

generation. However, a capacitance reduction of approximately 15% from that of the previous generation is required in the 65 nm generation.

Sony developed a porous organic film (porous PAE) with an optimized pore density and a second-generation SiOC/SiC layered process as a hybrid low dielectric constant film structure that can achieve the target performance.



■ Figure 2 Hybrid Dual Damascene Copper Wiring Cross Section



■ Figure 3 Wiring Capacitance Simulation Comparison

Dual Damascene Formation Methods

Sony developed the triple hard mask method as the new dual damascene formation method that supports the fine pattern formation required by the 65 nm generation. Figure 4 shows the layered PAE/SiOC film hybrid dual damascene formation method. As compared to the conventional dual hard mask method, the triple hard mask method has the following advantages.

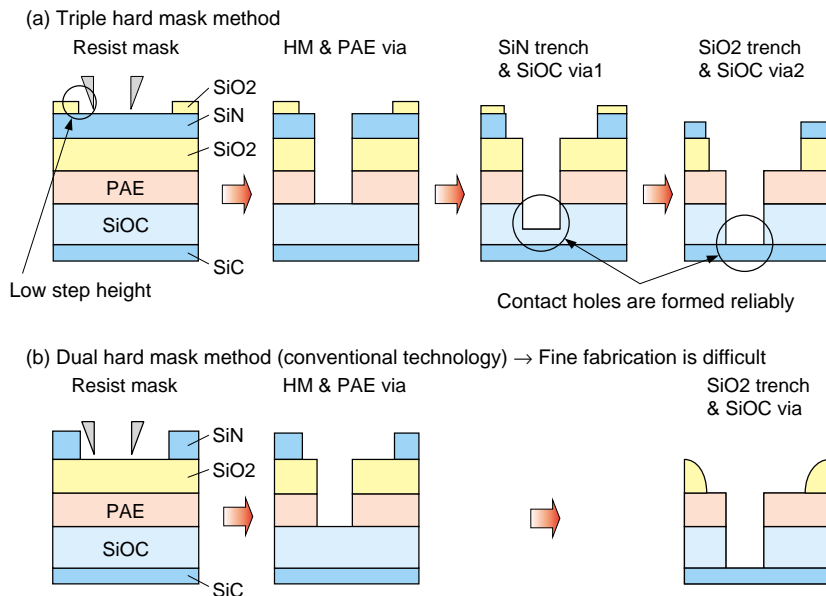
1. It improves the degree of contact hole fine fabrication precision to a level that can support the 65 nm generation by reducing the step height of the hard mask.

2. It makes easier to open holes in the SiOC film between contact hole interconnect.

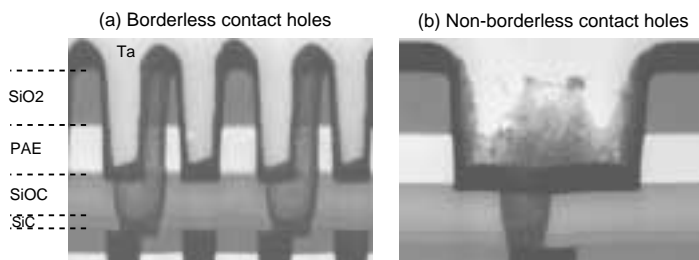
Photograph 1 shows the manufactured morphology of PAE/SiOC hybrid dual damascene fabricated using the triple hard mask method. Introducing this process allowed Sony to achieve a PAE/SiOC structure fine dual damascene fabrication that would have been difficult with conventional dual hard mask methods.

In addition, Sony developed the following technologies: low dielectric constant film formation optimal for a hybrid structure that can support the 65 nm generation, WET (postprocessing), copper embedding, and copper chemical/mechanical polishing, and also integrated these technologies into the fabrication process.

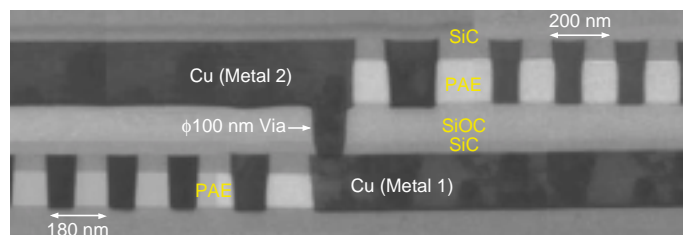
Photograph 2 shows the cross section of the completed hybrid dual damascene copper wiring. This photograph proves that this method can form 100 nm half-pitch multilevel wiring with excellent morphology for the first time in the industry.



■ Figure 4 Hybrid Dual Damascene Formation Methods



■ Photograph 1 Morphology due to Hybrid Dual Damascene Processing Using the Triple Hard Mask Method



■ Photograph 2 Cross Section of the 65 nm Generation Hybrid Dual Damascene Two-Layer Copper Wiring

Wiring Characteristics and Reliability

Table 2 presents representative electrical and reliability characteristics for PAE/SiOC hybrid dual damascene copper wiring. Sony verified that this process produces low-resistance high yield wiring and contact hole conductance characteristics with minimal sample-to-sample variations. Sony was also able to prove that this technology produces multilevel wiring with excellent resistance to heat for the thermal histories expected in the wafer process.

Superiority of Hybrid Dual Damascene

Table 3 presents the results of comparing the multilevel wiring structures assumed for the 65 nm generation. In addition to this newly-developed hybrid process, Sony also considered adopting the dual damascene structure that uses a single low dielectric constant film or the single damascene structure in which contact holes and wiring are formed separately. Based on a comprehensive evaluation of wiring performance, ease of implementation, and cost, of all these structures, the hybrid dual damascene structure is currently seen as the optimal process as a solution for the issues expected to face the 65 nm generation.

Future Development

Sony is now engaged in process optimization for the start of mass production, aiming at the completion of development by spring 2004 for 65 nm generation ultrahigh speed embedded DRAM logic. Sony also hopes to apply this leading-edge process module that includes multilevel wiring technologies to CMOS derived devices in addition to embedded DRAM logic. Sony is committed to continuing to contribute to the creation of new process solutions. Keep your eye on Sony for the latest CMOS process technologies.

■ Table 2 Hybrid Dual Damascene Wiring Electrical Characteristics/Reliability

	Yield	Resistance	Capacitance	Leakage current	Heat resistance
Wiring characteristics L/S = 100/100 nm	Over 95%	207 mΩ/□ Under ±15%	170 fF/mm Under ±15%	Under 1E-11 A/m	4 cycles at 400°C with no failures
Contact hole characteristics φ100 nm	Over 95%	1.5 Ω/via Under ±20%	—	—	4 cycles at 400°C with no failures

■ Table 3 65 nm Generation Low-Dielectric Constant Film Structure Copper Wiring Process Comparison

Process	Hybrid dual damascene structure	Single low-dielectric constant film dual damascene structure	Single damascene structure
Performance	◎	○	○
Difficulty	○	×	△
Cost	○	○	×
Overall evaluation	○	△	△

◎ : Excellent, ○ : Good, △ : Fair, × : Bad