FEATURING

The LEEPL Technology Promises to Solve the Crisis in Fabrication Facing the Semiconductor Industry

Next Generation Low-Cost Electron Beam Lithography Fabrication Technology

- **Simple exposure system**
- **Mask technologies that hold the key to practical application**
- **Constructing a multi-layer resist process**
- **Adoption of a die-by-die alignment method**
- **Achievement of 65 nm patterns**

Semiconductor fabrication technology, which must respond to market needs for higher performance and lower power consumption, is advancing more rapidly every year, and Sony's semiconductor development roadmap (see figure 1) has been moved up again. The development of 70 nm generation technologies, which will support the generation after next, is currently in progress. While several candidates for the fabrication technologies that will follow the 70 nm generation have been proposed, most of these technologies will require long development times, large research investments, and extremely expensive equipment. (See table 1.)

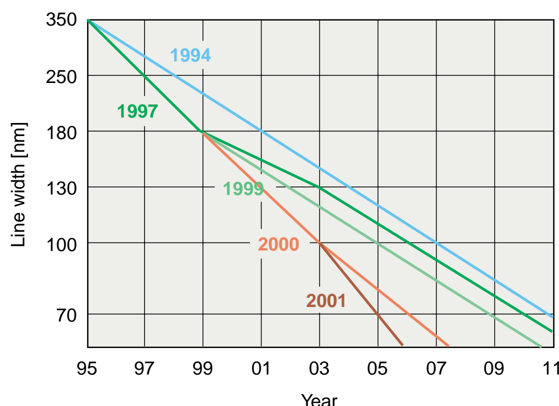
Sony has been focusing on the LEEPL technology, which features the use of low-energy electron beams and, with its low equipment costs and possibility of a short development period, may be able to resolve the next generation fabrication technology crisis facing the semiconductor industry.

LEEPL is abbreviation for low-energy electron beam proximity projection lithography, a lithography technology using low-energy electron beams developed by the LEEPL Corporation, a subsidiary of TOKYO SEIMITSU Co., Ltd. Normally, the circuit pattern is formed by exposure onto a photosensitive resist applied to the surface of the wafer in a lithography process. In LEEPL, a 2 keV low-energy electron beam is used as the light source for this exposure. This method has the following advantages: a high-resolution resist image can be acquired, throughput can be increased since it allows the use of high-sensitivity resist materials, and equipment costs are reduced due to the simple structure of that system.

This article presents an overview of the LEEPL technology and Sony's efforts in this area.

Simple Exposure System

In LEEPL, the mask used for exposure is the same size as the pattern exposed on the wafer. Also, the electron optical system is quite simple, as shown in figure 2 (a). The electron beam emitted from the electron gun passes through a deflector thus becoming a parallel electron beam. The electron beam made parallel by the deflector passes through a mask and forms an image on the wafer. Figure 2 (b) shows the electron optical system of the EPL method (EB stepper), which uses the same electron beam as LEEPL does for exposure. However, as can be seen from the figure, LEEPL has a far simpler structure. Compared to other NGL (next generation lithography) technologies, such as F2 lithography and EPL lithography, due to its simple structure, the LEEPL technology is expected to reqire a far shorter development time. In particular, alpha and beta prototype units have already been produced and evaluation is currently under way. Furthermore, the first production unit is planned to be in operation by spring 2003.



■ Figure 1 Semiconductor Roadmap Acceleration

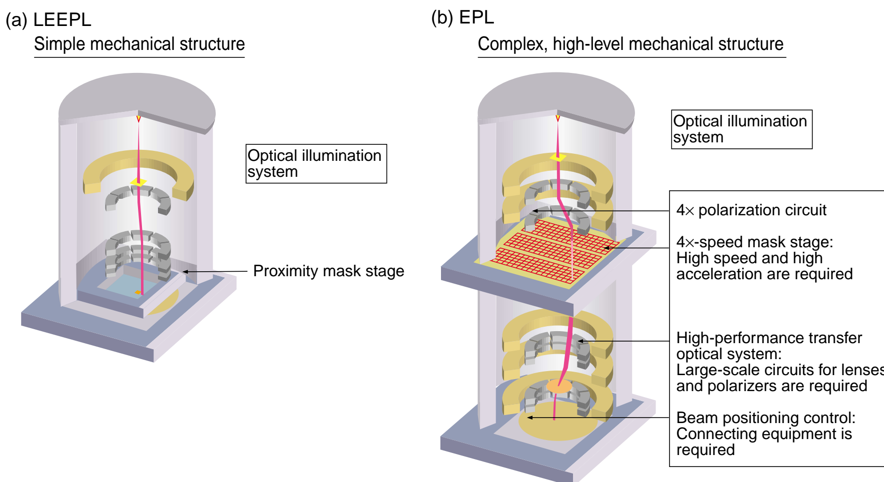
■ Table 1 Next Generation Lithography Technologies Comparison

Method	Light source	Market appearance timing	Issues for practical application
F2	157 nm laser	CY in fourth quarter 2003	Glass birefringence, resist materials
LEEPL	2 keV Electron beam	Beta equipment January 2002	1:1 masks, mask contamination
EPL	100 keV Electron beam	Beta equipment Second quarter 2003	Complicate exposure control system
EUV	13.5 nm EUV exposure	Beta equipment Fourth quarter 2004	Complicate exposure units, light sources, resist materials

Mask Technologies that Hold the Key to Practical Application of LEEPL

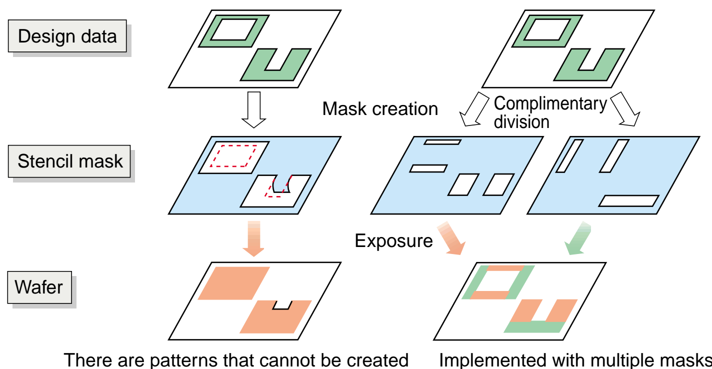
LEEPL uses a gap of about 50 μm between the wafer and the mask and exposes the wafer at a 1:1 magnification using real-size proximity projection. The masks used in the current mainstream technology, the stepper technique, are created with dimensions four or five times the actual dimensions of the wafer image. Since the design rules will be reduced even further in moving to the 70 nm generation, this means that LEEPL requires at least five times the mask precision of the current technologies. Furthermore, since, unlike light, electron beams cannot pass through matter, LEEPL uses stencil masks that are made by cutting holes in materials such as Si, diamond, or SiC.

Since patterns such as the closed figures shown in figure 3 cannot be formed in a stencil mask without the enclosed section falling out, a “complementary division technology” that divides the pattern into two or more patterns is required. Sony has proposed two types of complementary beam mask as shown in figure 4 (a) to achieve both the division into complementary components and the precision required in the mask. In this article, we introduce the complementary beam mask using one of these two types as an example. In the complementary beam mask, the exposure area is divided into four quadrants in which the orientation of the beams is different. Each of those quadrants is then divided further into small areas approximately 1 mm in size. These small areas are bounded by beams, exist independently, and are designed so that physical forces from other areas cancel out. The device pattern required to create the actual semiconductor chip is, after division into complementary areas, divided and placed in two quadrants chosen from the four quadrants. The device pattern is then formed on the wafer by exposing the four quadrants. The device pattern is reproduced on the wafer by exposing the four quadrants. This is shown in figure 4 (b). Although it would seem from this description that two quadrants would suffice, since the beams are present, there are places where patterns cannot be formed. Thus exposure of all four quadrants is required. Figure 5 shows a complementary quadrant beam mask that was created as a prototype.

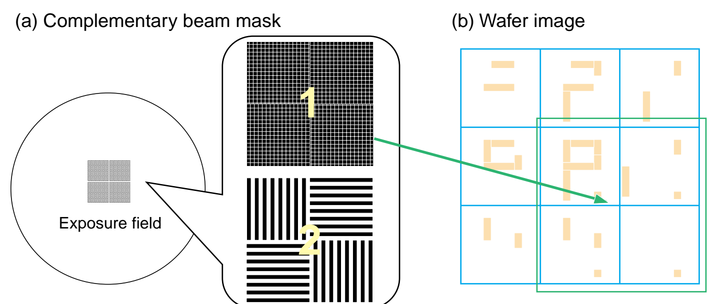


■ **Figure 2 LEEPL and EPL Electrooptical Systems Comparison**

■ **Figure 5 Four-Quadrant Complementary Beam Mask**



■ **Figure 3 Complimentary Division Technology**



■ **Figure 4 Complementary Beam Mask Proposed by Sony and its Wafer Image**

Constructing a Multilayer Resist Process

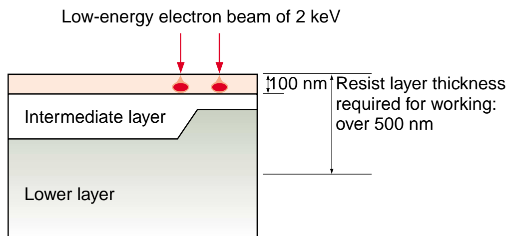
LEEPL uses an electron beam with an extremely low energy of 2 keV. This means that the electron beam used for exposure can only penetrate to a depth of approximately 100 nm, as shown in figure 6. In normal semiconductor processes, a film thickness of at least 500 nm is required for single resist layer operations to assure adequate resistance to etching of the foundation. For this reason, devices cannot be created in a single-layer resist process using wafers exposed by LEEPL, thus two-layer or three-layer multilayer resist technologies are required.

Multilayer resist process technologies were developed over 10 years ago to overcome the insufficient etching resistance of resist materials. Techniques such as the three-layer, two-layer, and silylation techniques shown in figure 7 were developed, and these technologies make it possible to create devices even in a structure with inadequate etching resistance by sequentially processing the wafer based on the pattern formed in the thin-film resist in the uppermost layer.

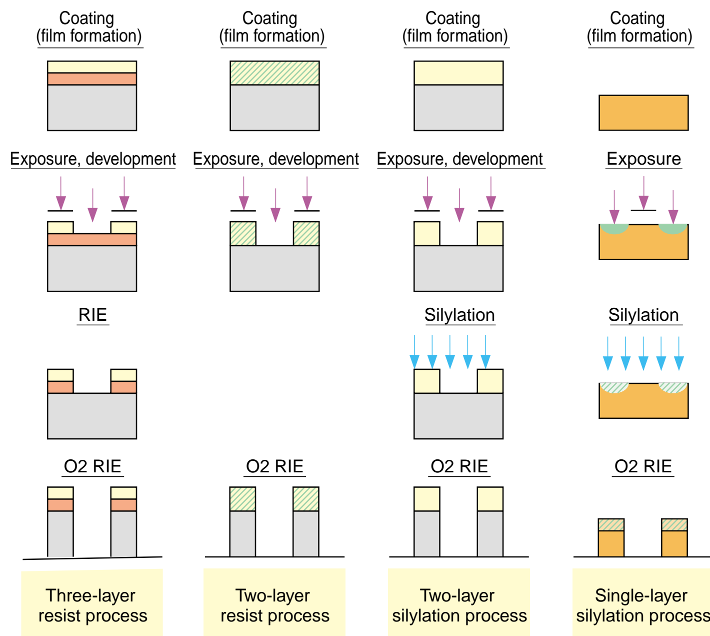
Sony is committed to implementing the LEEPL technology and proceeding with development directed at the 70 nm generation. As shown in figure 8, Sony is close to achieving a 70 nm pattern resolution in a three-layer resist process, and a 100 nm pattern resolution in a two-layer resist process. The current status is that we have essentially achieved a resolution that can be used in the 100 nm and 70 nm node semiconductor processes that will be used in future mass production.

Adoption of a Die-by-Die Method that Allows Correction at Each Shot during Alignment

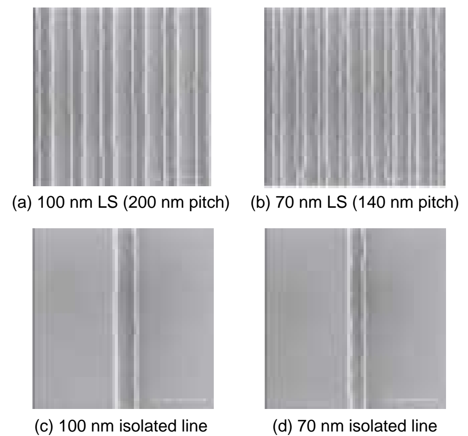
It is said that the required alignment precision for the 70 nm generation will be 25 nm. Precision above that used in current steppers is required in exposure methods such as LEEPL that require complementary alignment technologies. A die-by-die alignment method that uses diffuse white light is adopted in LEEPL. The positional displacement is measured by calculating the relative positions of the mask and the wafer from the peak posi-



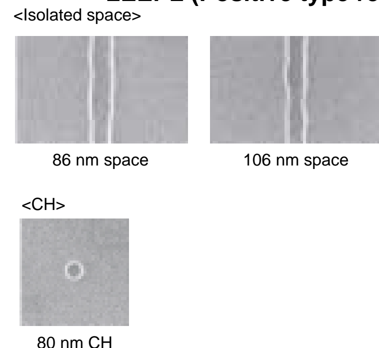
■ **Figure 6 Electron Beam Behavior in the Resist**



■ **Figure 7 Process Flows that Support LEEPL**



■ **Figure 8-1 Resolution of Resists that Support LEEPL (Positive type resists)**

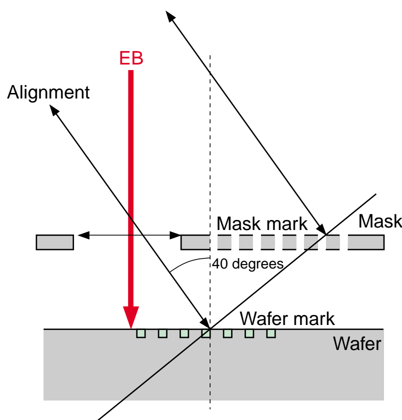


■ **Figure 8-2 Resolution of Resists that Support LEEPL (Resists that support multi-layers)**

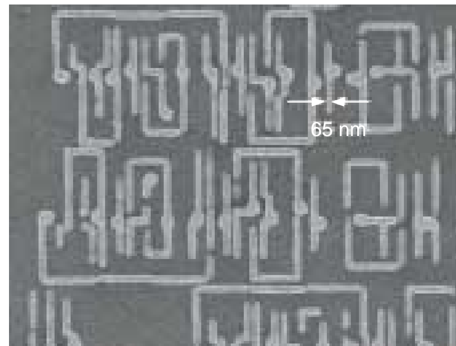
tions of the signal from the wafer mark and the signal from the mask mark as shown in figure 9.
Correction is performed for each shot from the positional displacement information measured in this way, thus achieving a high-precision alignment. The offset, rotation, and magnification can be corrected for each wafer and shot in the same manner as in current steppers. Additionally, the gap between the mask and wafer is measured continuously, eliminating resolution degradation due to defocusing of the electron beam. Performance capable of achieving a 30 nm alignment precision has already been verified, and Sony is now aiming at improving precision even further to put this technology to practical use in the future.

The Consortium and the Outlook for LEEPL Technology in the Future

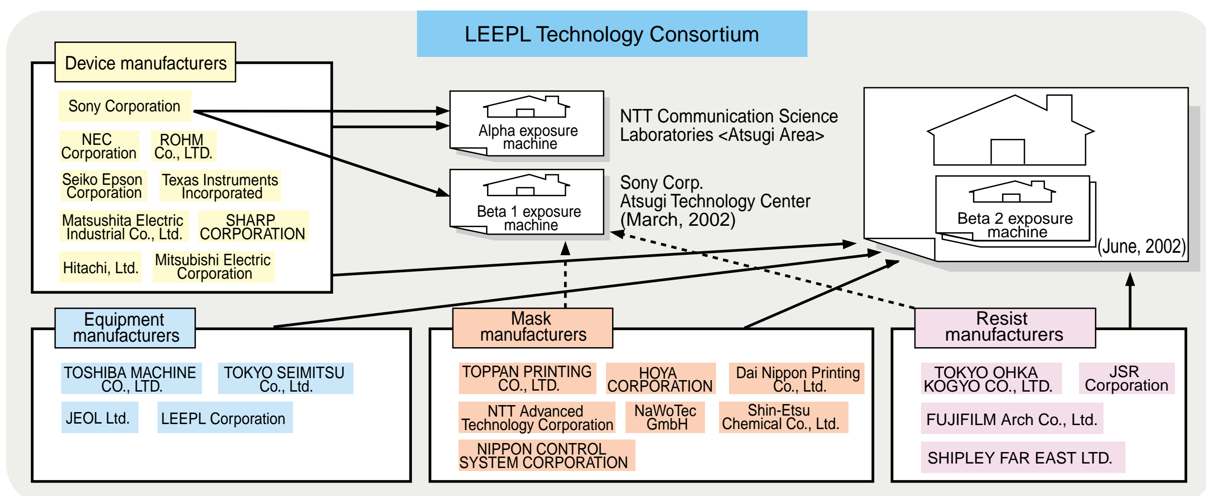
LEEPL technology development at Sony consists of the development of the equipment, mask, process, and alignment technologies introduced here and the current status is that Sony has already succeeded in complementary exposure of 65 nm device patterns. (See figure 10.) In the near future, Sony will be working to increase the completeness of this technology by proposing new formats, using existing technologies, and other means, all aimed at practical application of the LEEPL technology. The LEEPL Technology Consortium was formed in June 2001 by 14 companies, including device, mask, resist, and equipment manufacturers to promote the development of the LEEPL technology. This consortium now consists of 24 companies. (See figure 11.)
Consortium activities include development and technology standardization activities aimed at achieving practical application of LEEPL through laboratory testing and evaluation at the Hachioji facilities of TOKYO SEIMITSU Co., Ltd.
Sony is working on developing next generation process technologies to allow the manufacture of chips with even higher performance and integration densities at lower cost. With respect to fabrication technologies, which correspond to a major component of the costs in semiconductor processes, Sony is committed to promoting the practical application of LEEPL technology. Keep your eye on Sony semiconductors for the latest developments and technologies.



■ **Figure 9 Alignment Optical System that Supports LEEPL**



■ **Figure 10 Device Pattern Implemented with a Complementary Mask**



■ **Figure 11 LEEPL Technology Consortium**