Techno World

Sony's Leading Edge Package Technology for System LSIs

Packages for High Density Mounting

- **Combining of substrate mounting and semiconductor mounting technologies**
- **From package innovation to system innovation**
- **Minimization of total costs**
- **Development of environmentally friendly packages**

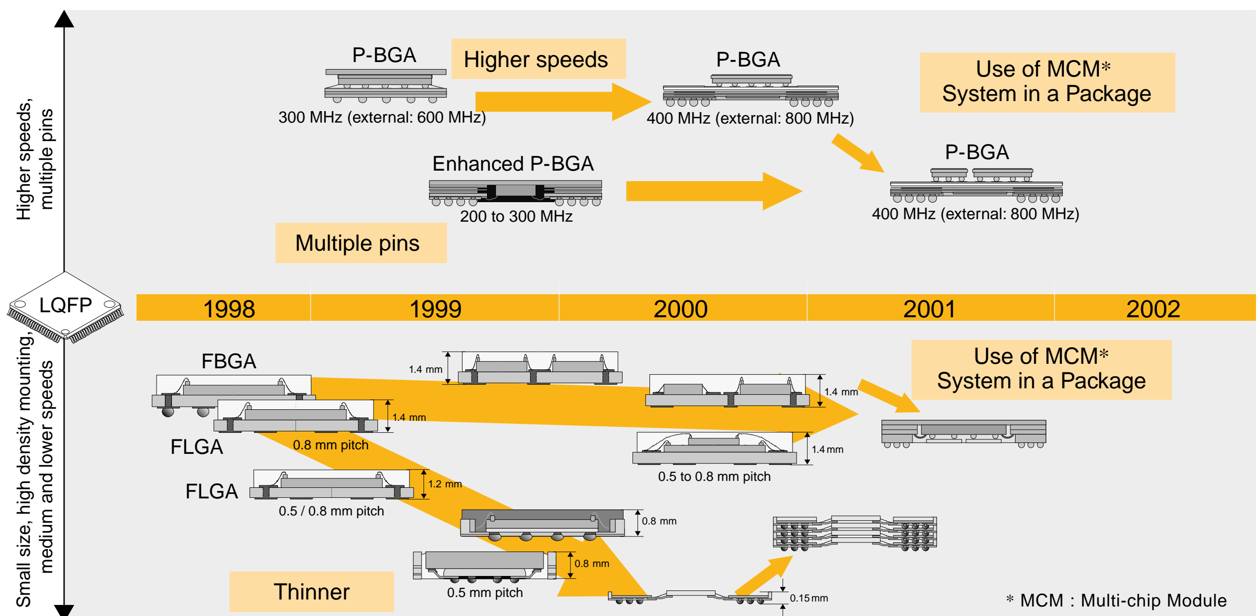
Rapid progress is now being made in the development of large-scale system LSIs to achieve further miniaturization and lighter weights, increased functionality, and higher performance in digital home information appliances. Semiconductor mounting technology is a critical key technology for creating these large-scale system LSIs.

Although the term "mounting technology" strongly implies the conventional technologies for mounting on a mother board or other printed circuit board, such as Surface Mounting Technology (SMT), it has recently come to be used in a wider sense to also refer to the so-called "system integration technologies" that take full advantage of semiconductor fabrication technologies. These include technologies for "bump" formation and rewiring on the chip itself, and technologies for machining wafers down to sheet-like thicknesses and laminating them together in multiple layers.

In this article, we introduce two Sony semiconductor mounting technologies: small thinner package as represented by the Chip Size Package (CSP) technology, and single-package implementation technologies that incorporate multiple LSI chips and passive components such as LCR (inductors, capacitors, and resistors) in a single package, as represented by System in a Package (SiP) technologies.

Package Development Roadmap

Figure 1 shows Sony's roadmap for package development. The purpose of the semiconductor package is to interface cleanly to the mounting substrate (PCB) and to maintain the electrical characteristics of the device. In conjunction with the higher functionality and increasing miniaturization seen in contemporary electronic products, device characteristics are being improved continuously and device packages must preserve those improved electrical characteristics. At the same time, since mounting densities on mounting boards are increasing, the added value provided by the packages themselves is increasing. Within these trends, and while keeping environmental



■ **Figure 1 Package Development Roadmap**

concerns in mind, many packages and packaging concepts have been proposed.

The form of package has shifted radically, from the conventional pin insertion type to the surface mounting type, and the Ball Grid Array (BGA) package has become the representative package for high-speed multi-pin devices. As compared to the fine-pitch QFP, the BGA has the rather wide external lead pitch of 1.27 mm. The resultant ease of mounting has led to its wide adoption. The two main techniques for chip connection are wire bonding and bump connection. The former features improved radiation characteristics and is used for low cost devices with over 300 pins, and the latter is appropriate for improving characteristics in the high-frequency area and allows the lengths of connections to be minimized. The latter is adopted as the package for contemporary high-speed SRAM products.

In the small high-density package area there has been significant progress in the development of the CSP package type, which features package dimensions as close as possible to those of the chip itself and an external lead pitch reduced to 0.8 mm or narrower. Recently, there has been demand for even thinner form factors, and in addition to the transition from the conventional wire bonding to bump connection, there has also been progress in the development of three-dimensional laminated packages in which the wafer is made into a thin sheet.

In the future, Sony will expand its lineup of high-speed multi-pin packages that include multiple LSIs as well as developing packages that include passive components for MCMs to support increased functionality levels in individual packages.

Small Thinner Packages

1. Flip-Chip Type <FC-BGA>

Figure 2 shows a typical small package for bump connection devices that uses an interposed organic substrate. In high-speed large-scale 0.25 µm generation system LSIs, if conventional wire bonding connection was used, the reduction of the voltage between power supply and ground during low-voltage operation due to the influence of the inductance due to wire lengths and chip internal wiring would be significant and could cause the chip to malfunction. One method for resolving this problem is the use of bump connections, and a wide range of manufacturing techniques have been proposed. Packages that use this bump connection technique are expected to become an increasingly important technology due to the trends towards lighter, thinner, smaller, and faster electronic equipment. This technology is expected to be used widely in many areas. However, it is clear that the creation of a Pb-free low-cost bump formation technology will become an important issue in the future.

2. Packages Using UFPL

The Ultra-Fine Pitch Lead frame (UFPL) was developed as an interposer for small thin packages, and a unique Sony technology.

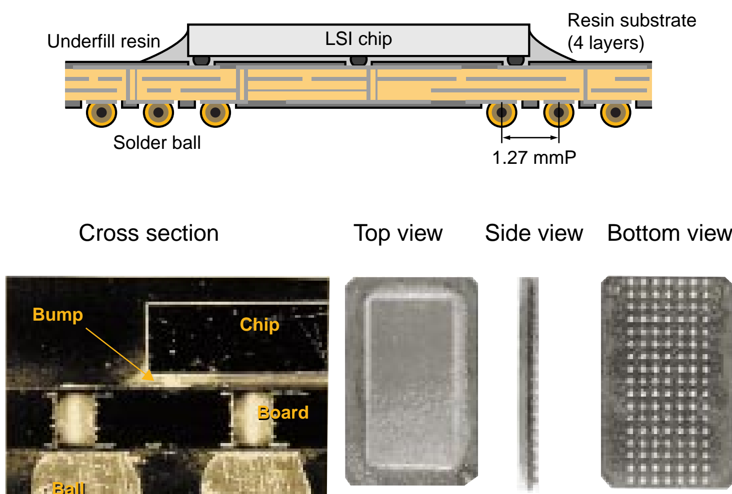
The UFPL has the following five features.

- Cu wiring pattern formation by electroplating
- Package formation by etching
- Polyimide insulation layer formation by etching
- Metal core ball formation by electroplating
- Bump formation on the lead tips

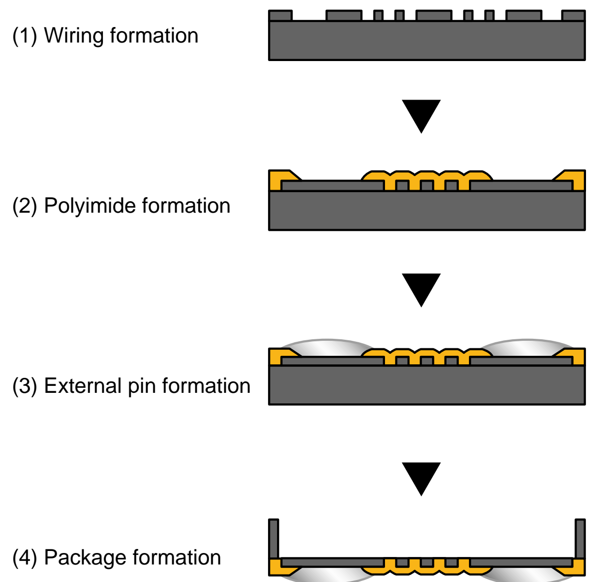
Figure 3 shows the UFPL manufacturing process.

(1) Wiring formation

A copper alloy material with a thickness between 100 and 150 µm is used as the base material, and the conductor pattern is formed as Au-Ni-Cu wiring by an electroplating technique. Unlike etching techniques, this technique



■ Figure 2 FC-BGA(Flip Chip-Ball Grid Array)



■ Figure 3 UFPL Manufacturing Process

allows the creation of patterns with line and space widths of 20 µm and 20 µm, respectively.

(2) Polyimide formation

Next, the support layer of the conductor pattern is formed independently. This allows the insulating material to be selected according to needs for a thinner or application.

(3) External pin formation

Au/Ni external pins (bumps) are formed by electroplating on open sections of the polyimide layer. This allows the formation of pins at pitches finer than is possible with ball mounting techniques.

(4) Package formation

The unneeded sections of the base material are then removed by etching, completing the structure as an interposer. Furthermore, one significant advantage of the UFPL technique is that this base material may be retained as an outer lead or a strengthening material.

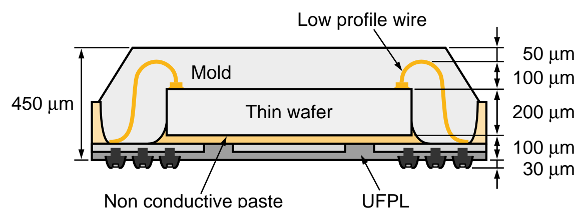
Figure 4 shows a thin package with a height of 0.5 mm using this UFPL technique. Packages of this type can be mass produced using conventional production lines and assembly techniques. Thus UFPL is a superlative technique which may be applied in a wide range of application as described above.

System in Package

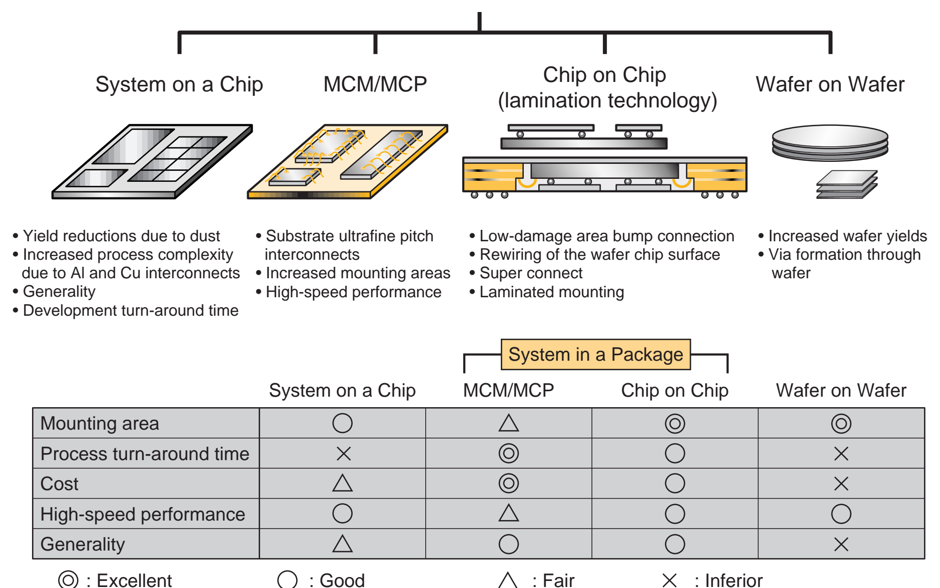
Techniques such as those shown in figure 5, implementation as a single chip, MCM/MCP, Chip on Chip lamination, and Wafer on Wafer lamination, are possibilities for implementing large-scale system LSIs. Of these, implementation as a single chip is seen as the mainstream, and it is this approach that has been studied the most. Implementation as a single chip refers to the formation of a system or a subsystem as a single LSI that integrates multiple functions on a single chip, taking CPU, memory, logic, and even software modules as core elements. However, this technique suffers from several problems, including yields being reduced by every defect in each individual block, a more complex manufacturing process, longer turn-around times, and higher development costs. As a result, the current status is that while it is technologically feasible to create single chips that use differing processes, such as analog, digital, and power system technologies, it remains problematic economically. As a result, implementing systems in a single package has been receiving increased attention recently.

There is now a lively debate concerning the realization of large-scale system LSIs. In particular, should they be created by forming all systems on a single chip (System on a Chip - SoC), or should they be created by forming all systems in single package (System in a Package - SiP). We expect that these two approaches will find their respective application areas in which their respective strengths can be taken full advantage of.

Sony recognized these issues in the implementation as a single chip approach from an early point, and, for example, in 1999, manufactured both 2-in-1 and 3-in-1 package products that provided identical performance to single chip implementations that combined leading edge logic LSI and general-purpose DRAM for use in MD Walkman products. (See figure 6.) Sony is also manufacturing 2-in-1 package product with the same package size



■ **Figure 4 UFPL thin Package**



	System on a Chip	MCM/MCP	Chip on Chip	Wafer on Wafer
Mounting area	○	△	◎	◎
Process turn-around time	×	◎	○	×
Cost	△	◎	○	×
High-speed performance	○	△	○	○
Generality	△	○	○	×

◎ : Excellent ○ : Good △ : Fair × : Inferior

■ **Figure 5 Implementation of Large-Scale System-on-Chip LSIs**

as LQFP products using the UFPL technique described above, as shown in figure 7.

One other issue in positioning SiP products as described above, is packages that also include passive components, such as LCR (inductors, capacitors, and resistors). Sony is well aware of this issue as well, and will be providing packages that combine both semiconductor and board mounting technologies.

Wafer Thinning and Lamination Technologies

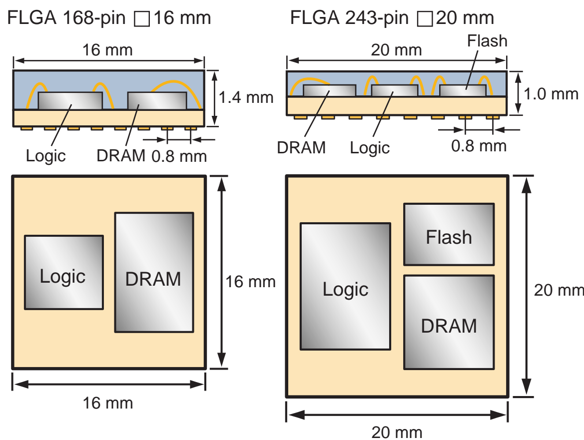
In developing thin laminated packages, the basic technology involved is the technology for thinning wafers. Photograph 1 shows the result of machining the back side of an 8-inch wafer to trim it to a thickness of 50 µm. Wafers are normally thought of as flat, but when machined to a thickness of 50 µm, they often acquire a significant amount of warp. On a wafer, the interlayer insulating film and the interconnect layers have residual stresses, and the relationship with the underlying silicon causes warping. Figure 8 shows a 200 µm ultra-thin package using these thin wafers. However, full and complete device characteristics evaluations are required before these can be released as commercial products.

Sony is also developing a three-dimensional lamination technology as the next generation of MCM technology. Sony is developing this technology to both reduce mounting area and support multiple chips in a single package, and is currently targeting this technology for increasing Memory Stick™ capacity. Of course, making each layer as thin as possible is important for lamination, and Sony is developing thinner technologies in addition to these lamination technologies.

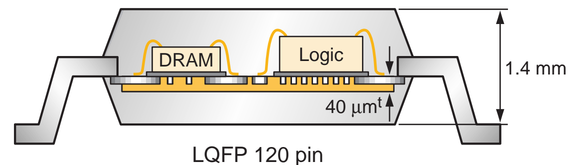
Figure 9 presents an 8-stacked laminated flash memory using these technologies. The thinner technologies involved here include both machining 8-inch wafers to a 50 µm thickness as well as thinning the interposed layers used for extracting the internal electrical signals to a mere 20 µm, resulting in a single layer thickness of 120 µm. As a result, we achieved an 8-stacked laminated device with a thickness of 1.0 mm. The interposed layers used here are the UFPL described above. In these layers the circuit formation sections have a thickness 20 µm, and the surrounding 100 µm thickness reinforcing material sections are formed at the same time as the circuit sections.

Future Developments

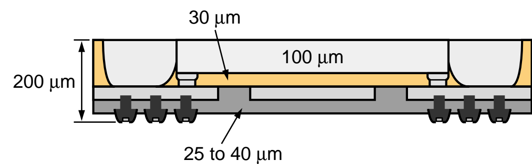
As device design rules move to the quarter micron and lower range and wafer processes change radically, the electrical characteristics requirement on device packages are becoming increasingly strict. Within this context, Sony is committed to continuing to provide our customers with leading-edge packages intimately linked with semiconductor technologies and customer needs with respect to cost, size, electrical characteristics, thermal characteristics, mounting characteristics, and reliability.



■ Figure 6 Multiple Chips in an FLGA Package

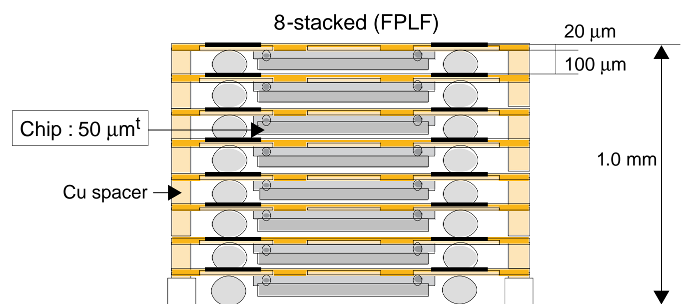


■ Figure 7 Multiple Chips in an LQFP Package



■ Figure 8 Ultra-Thin Package

■ Photograph 1 Wafer with a 50 µm Thickness



■ Figure 9 8-Stacked Laminated Package