Techno World

Leading-Edge LSI Process and Device Technologies for Networked AV and IT Products

0.13 µm Process and Device Technologies

- **New gate structure**
  Micro-fabrication of W/WN/poly-Si stacked gate devices
- **Multilevel wiring using Cu and low dielectric constant materials**
  Dual-Damascene process for lower power.
- **Single-wafer spin cleaning with repeated use of ozonated water and dilute hydrofluoric acid**
  High-performance environmentally friendly process
- **MONOS flash memory**
  Low voltage, scalable, and suitable for embedding in logic chips.

In the history of semiconductor device development, the competition to produce larger commodity DRAMs has driven increases in integration densities and the competition to produce faster CPUs has driven increases in logic speeds. These improvements have been achieved by progress in semiconductor fabrication process and device technologies.

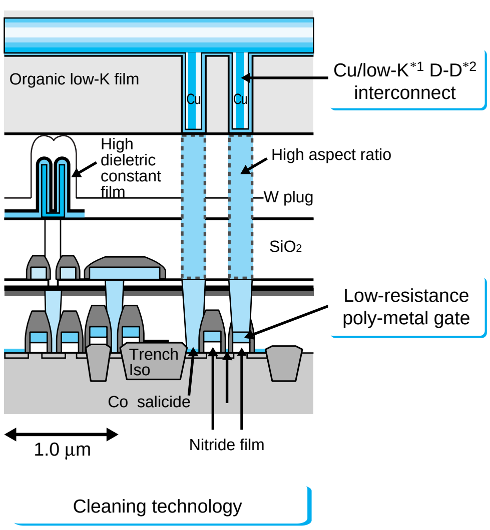
As this technology advances, Sony focuses on applying this technology to integrated AV and IT*1 products. In this area, high integration densities and high speeds are required to integrate the wide range of functions required in system LSI products, yet at the same time reduced power consumption is required for portable applications. Devices that can be scaled to narrower design rules are critically important keys to achieving this performance.

The size of the design rules in each process technology generation is seen as the measure of the technology used to fabricate MOS semiconductor devices.

Now, the fierce competition between high-speed CPU manufacturers is accelerating the progress of technology generations.

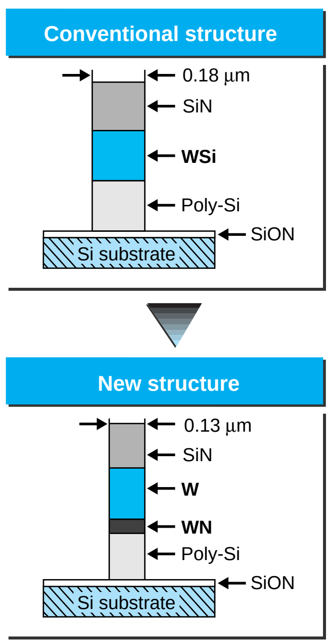
Sony has already developed embedded DRAM technology for system LSI devices at both the 0.25 µm and 0.18 µm generations, and is committed to improving this technology even further to allow the integration of an even wider range, and an even larger number of functions in 0.13 µm generation devices. This article presents the Sony-developed technologies for the 0.13 µm generation shown in figure 1.

- Transistor gate electrode formation technology — the key technology in the front end stage of the fabrication process
- Dual-Damascene interconnect technology — an indispensable technology in the back end stage of the fabrication process. This technology is based on the use of copper and a low dielectric constant interlayer film.



*1 Low-K : Low Dielectric Constant
*2 D-D : Dual Damascene

■ **Figure 1 0.13 µm Generation MOS LSI Structure**



■ **Figure 2 Gate Electrode Structure**

- A new cleaning technology that achieves high performance, is environmentally friendly, and is used many times during the LSI fabrication process
- MONOS*2 flash memory, which allows the feature sizes of both the logic circuits and the flash memory on the same chip to be scaled down.

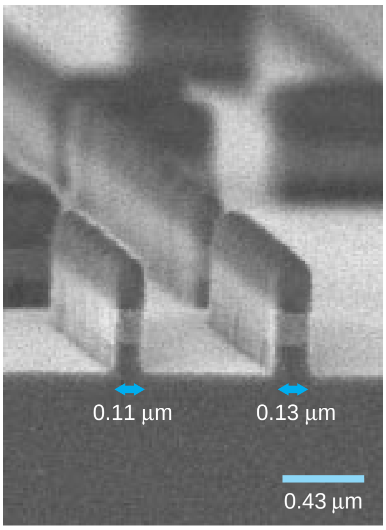
*1 IT: Information technology
*2 MONOS: Metal oxide nitride oxide semiconductor

New Gate Structure for the 0.13 µm Generation Transistor

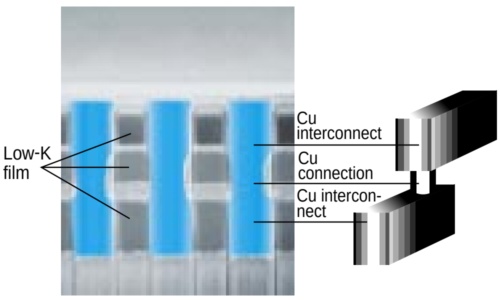
While the 0.13 µm generation transistor is characterized by a gate length of a mere 0.13 µm, an even narrower 0.10 µm gate will be necessary to provide even higher speeds. In these radically scaled down transistors, it is no longer possible to ignore the gate resistance. To achieve higher speed, we must reduce the resistance of the gate electrode. To do this, we must reduce the resistivity of the gate electrode. This also results in a lower aspect ratio which makes it easier to form the self-aligned contact in the DRAM Cell. Although conventional WSi/poly-Si electrodes have had a sheet resistivity in the range 15 to 20 Ω/□ , a sheet resistivity of 5 Ω/□ or less is required in this new generation. To solve this problem, Sony is investigating the use of a so-called poly-metal electrode that has a W/WN/poly-Si structure using tungsten (W) itself instead of WSi. (See figure 2.) Previously, high-temperatures have been required in the etching processes used for creating metallic W patterns on ICs. However, Sony has now developed a novel room-temperature etching technology for precise gate formation in this new W electrode structure. As shown in figure 3, this allows the creation of an ultraminiature gate that can support the 0.10 µm generation transistor. We have also verified that the sheet resistivity of the gate electrode has been lowered to 1.7 Ω/□.

Copper/Low Dielectric Constant Interconnects

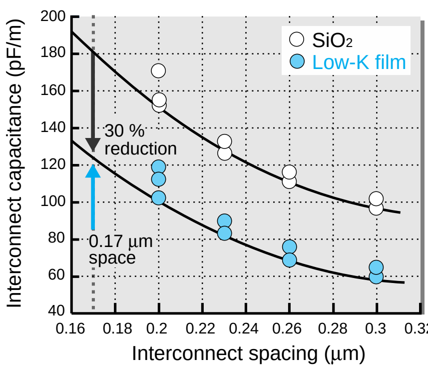
In ultrahigh integration level semiconductor devices, not only must the interconnects be made narrower, they also must be spaced more closely with the scaling of the device. Since it is not possible to use thicker interconnects, the current density increases inversely with the integration density, and the resistance of the interconnect material must be reduced accordingly.
At the same time, since the interconnect spacing is reduced, the capacitance between pairs of interconnects increases, and makes it difficult to reduce power consumption at higher operating frequencies. For this reason, instead of aluminum (3.0 µΩ/□) and SiO_2, low-resistance copper (1.8 µΩ/□) and low-K interlayer dielectric materials are now used as the interconnect material. However, copper has the problem that it is difficult to etch. Therefore it is necessary to adopt a grooved interconnect structure (the Damascene method) in which grooves are formed in the interlayer dielectric between interconnect layers in advance, a copper layer is formed, and then the excess metal is removed using CMP*3. Sony will be adopting the so-called dual-damascene method, in which the interconnects and the connections between interconnect layers are formed in a single operation.
Sony and other manufacturers in the industry have investigated the use of a wide range of low dielectric constant (low-K) materials instead of the earlier SiO_2 (silicon oxide film) which had a relative permittivity of around 4.2 for the insulating film between interconnect layers. However, it was Sony who first demonstrated formation and etching technologies for an organic low-K material with a dielectric constant of 2.8 and excellent abilities to withstand heat. This etching process also has the advantage that it does not require the use of the environmentally damaging PFC*4.
Sony has succeeded, for the first time in the industry, in forming interconnects using a dual-Damascene technique that also forms the connections between interconnect layers at the same time by using the combination of copper and this organic low dielectric constant



■ **Figure 3 Formation of Poly-Metal Gate**



■ **Figure 4 Cu/Low-K Dual-Damascene Interconnect**



Low-K: Low dielectric constant

■ **Figure 5 Reduced Interconnect Capacitance due to Low-Dielectric Constant Film**

film. (See figure 4.) We have verified that this achieves a 30% reduction in the interconnect capacitance over earlier techniques. (See figure 5.) We have also verified that the resistance of the copper via plugs formed at the same time in this method is an order of magnitude lower than those in the earlier W connections.

*3 CMP: Chemical mechanical polish
*4 PFC: Perfluorocarbon

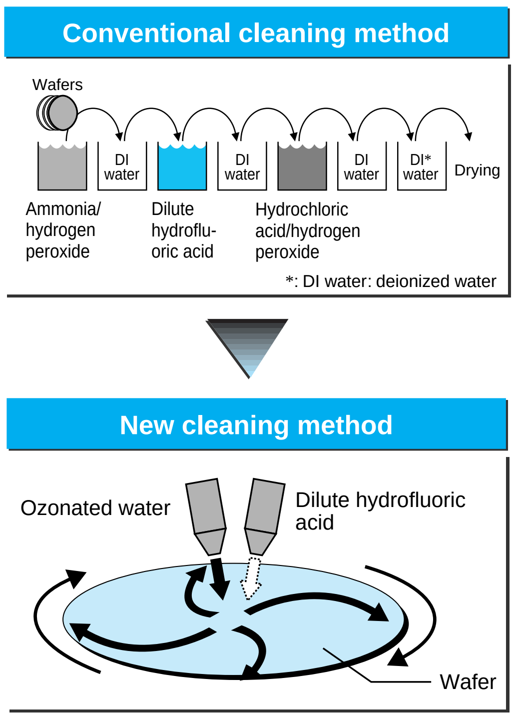
Single-Wafer Spin Cleaning with Repeated Use of Ozonated Water and Dilute Hydrofluoric Acid

Even higher degrees of cleanliness are required as the design rules used for semiconductor device fabrication are scaled down further and further. In conventional cleaning techniques, hazardous chemicals such as ammonia and hydrochloric acid are used in addition to dilute hydrofluoric acid and multiple wafers are immersed in a cleaning tank at the same time. In this method, contaminants removed from the wafers accumulate in the solutions and redeposition of contaminants makes achieving ultraclean wafer surfaces difficult. Also, as wafer diameters increase, the size of the tanks used for cleaning must also increase, resulting in the use of large volumes of chemicals and DI water. In particular, since DI water is used both to dilute the chemicals and to rinse them away, conventional techniques require extremely large volumes of DI water. Furthermore, since there may be as many as 100 cleaning steps in LSI fabrication, the amount of chemicals and DI water used is large enough to become a significant environmental problem. Thus from this standpoint alone, there is a pressing need to reduce the amount of chemicals required.

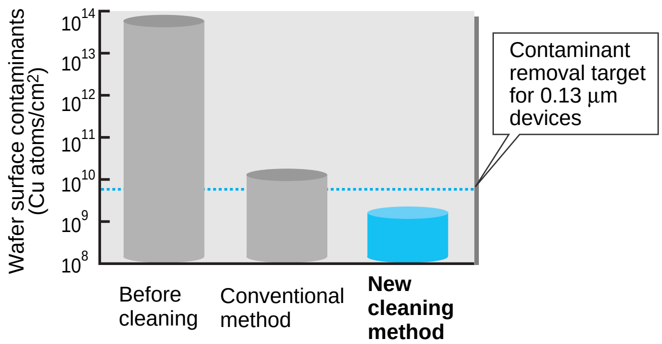
Sony has developed the novel cleaning method shown in figure 6. This technique alternately sprays dilute hydrofluoric acid and ozonated water for a few seconds each on the wafer as it is being rotated, and repeats this cycle. In addition to always using fresh chemicals and DI water and not using ammonia, hydrochloric acid, and other chemicals that damage the environment, this technique also allows the amount of chemicals and DI water used to be reduced. This technique can reduce the amount of metallic pollutants by one half, and can achieve the level of cleanliness required for 0.13 µm generation devices. (See figure 7.) We have also proved that this method reduces the volume of chemicals and DI water used to 1/20 that of conventional methods.

MONOS Flash Memory

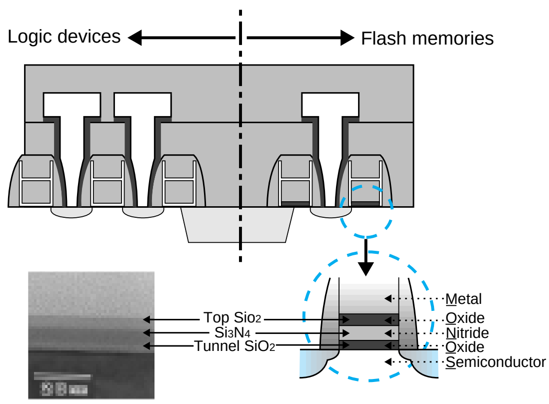
System LSI products must integrate many functions and devices on a single chip. In particular, the ability to include embedded DRAM and embedded flash memory along with logic is extremely important for many applications. At the same time, flash memory devices have now reached a scale where commodity FG*5 type products with 256M bits of memory are available in quantity. However, due to its structure, FG type flash memory requires a programming voltage of between 17 and 20 V. The inability to reduce this programming voltage makes it difficult to further scale down the FG type flash memory geometry and also makes it difficult to embed it on the same chip with logic



■ Figure 6 Comparison between Conventional and New Cleaning Methods



■ Figure 7 Removal of Metallic Contaminants Achieved by New Cleaning Method



■ Figure 8 Sealed Down MONOS Memory Structure for Embedded Use circuits.

Sony has now developed a MONOS type flash memory that supports lower programming voltages and thus both allows the use of scaled down fabrication technologies and can be more easily embedded in system LSI devices. (See figure 8.)

Unlike FG flash memory, in which the memory function is created by storing a charge on an electrically floating poly-Si gate, the MONOS type operates by storing charges on distributed carrier traps in an SiN (silicon nitride) layer. If there are local defects in the oxide film that the electrons pass through in the programming and erase operations, the FG type loses the majority of its stored charge through those local defects. However, this problem does not occur with the MONOS type because the traps are distributed. Thus the device retains the majority of its stored charge. As a result, it is possible to use thinner SiO_2 films in the MONOS type. This allows the programming voltage to be reduced and the design rules to be scaled down further. Furthermore, MONOS memory is advantageous for logic circuit embedded memory since its fabrication process is compatible with that of the surrounding logic devices.

Sony is studying the possibility of designing a single-transistor memory cell using the MONOS type flash memory device. One feature of this memory cell is that it would support fabrication in geometries scaled down to at least 0.10 µm rule processes. (See figure 9.) Furthermore, we have already shown that the MONOS type flash memory cell can be rewritten at least 10^6 times, ten times that allowed by the FG flash memory cell.

*5 FG: Floating gate

Future Development

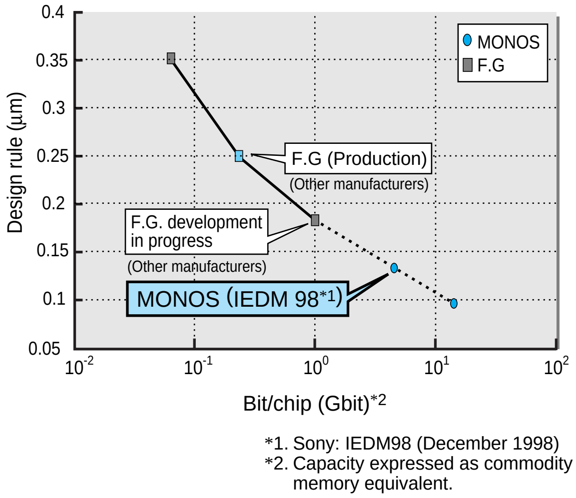
In this article we have presented a few of the individual technologies that will be used in the 0.13 µm generation. In particular, we have focused on certain technologies in which Sony has achieved important and significant results. However, there are still several fundamental semiconductor process technologies that must be developed or that require further advances. These include lithography for ultrafine patterns, the formation of high-reliability gate insulating films, and the formation of extremely shallow source/drain junctions.

In the near future, Sony must integrate these individual technologies and perfect them for use in volume production. Issues that arise here due to integration include achieving the required tradeoffs in dimensional precision between lithography and etching processes and minimizing changes in material properties and qualities due to repeated thermal processing. The difficulties that arise here are radically different from those faced in developing individual technologies. The key to overcoming these problems lies in providing adequate process margins to create a high-reliability, high-yield integrated process.

Sony is committed to overcoming these difficult technological problems presented by the 0.13 µm generation. By creating a high-performance process device technology, Sony hopes first to achieve a standard speed of 600 MHz, and then, by optimizing that process technology and reducing voltages, to create devices with even lower power consumption levels. We hope that devices in the 0.13 µm generation will incorporate on-chip DRAM or flash memory subsystems with around 256 M bits of storage.

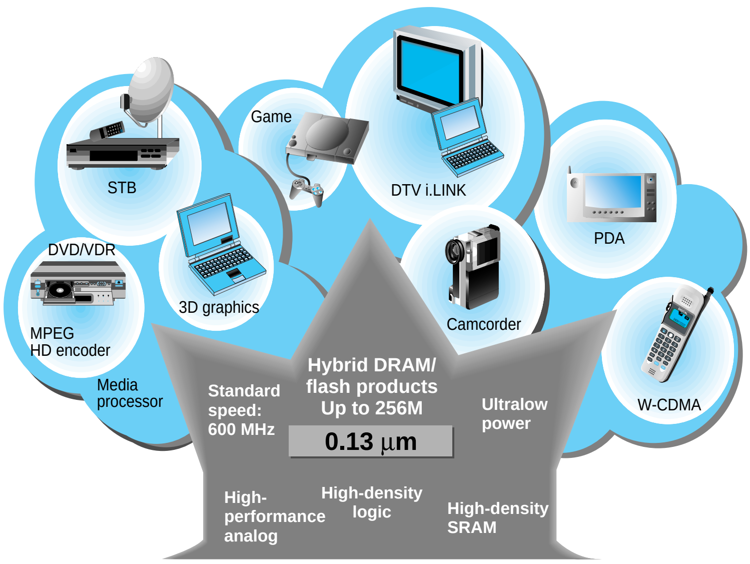
We firmly believe that this technology will support the creation of high-definition camcorders, digital TVs, and games, and that lower power consumption will contribute to high-definition PDA*6 products. (See figure 10.)

*6 PDA: Personal digital assistant



*1. Sony: IEDM98 (December 1998)
*2. Capacity expressed as commodity memory equivalent.

■ **Figure 9 Trends of Scaled Down in Flash Memory**



■ **Figure 10 Support of AV and Information Technology Products by 0.13 µm Process Technology**