PHS RF Front End Integrated in a Single Package
PHS GaAs MMIC

CXG1051AFN

The CXG1051AFN implements a PHS RF front end, a circuit which in prior systems was formed from two ICs, in a single package by adopting a two-chip single-package format.
This device adopts the ultraminiature HSOF26 package, which achieves a 0.4-mm lead pitch for the first time in the industry. The electrical characteristics of the device were also improved, in particular the current consumption was reduced and the distortion characteristics were improved. At the same time, this device achieves an ideal pin layout from the standpoint of signal flow, and thus is significantly easier to use.
Thus the CXG1051AFN can contribute to longer battery life and miniaturization in PHS terminals.

- **Single positive supply operation: V_{DD} = 3 V**
- **Miniature molded package: HSOF26**
- **Power amplifier/antenna switch transmitter block**
  - **Low current consumption: I_{DD} = 150 mA**
  - **High power gain: Gp = 39 dB (at 1.9 GHz)**
- **Antenna switch receiver block/low-noise donwconversion mixer**
  - **Low current consumption: I_{DD} = 5.5 mA**
  - **High conversion gain: Gc = 21 dB (at 1.9 GHz)**
  - **High image rejection ratio: IMR = 40 dBc**
  - **High 1/2 IF rejection ratio: 1/2 IFR = 44 dBc**

Two Chips in One Package

At the planning stage, we realized that there would be almost no chip area savings provided by integrating the power amplifier/switch block and the low-noise amplifier/mixer block on a single chip. Given that, we thought that the approach of housing two chips in a single package might be effective at providing improved characteristics and reducing costs at the same time. This is the approach we adopted in this product. (See figure 2.)

VOICE

To be honest, recently I've found myself wondering whether we were going to be able to actually complete many of the projects I've been involved in. Still, we've always succeeded in making it to mass production within our customers' desired time frames. In thinking about this, it seems to me that this demonstrates the superlative balance between Sony's technologies: the circuit technologies that include experience with all of the PA, SW, LNA, and mixer circuits used, the wafer technology that supports those circuit technologies, and also packaging technology. The CXG1051AFN corresponds to the condensation of all of Sony's current GaAs MMIC technologies.

Newly-Developed HSOF26 Package

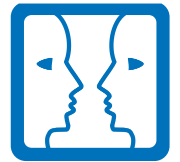
The 26-pin HSOF (small outline flat lead package with integral heat sink) package was developed specifically to make the CXG1051AFN a more powerful product. While the 0.4-mm lead pitch supports radical miniaturization, this package provides a reduced thermal resistance and achieves an ideal ground by exposing the die pad section of the lead frame at the back of the package. These play significant roles in allowing the chips to exhibit their characteristics fully.

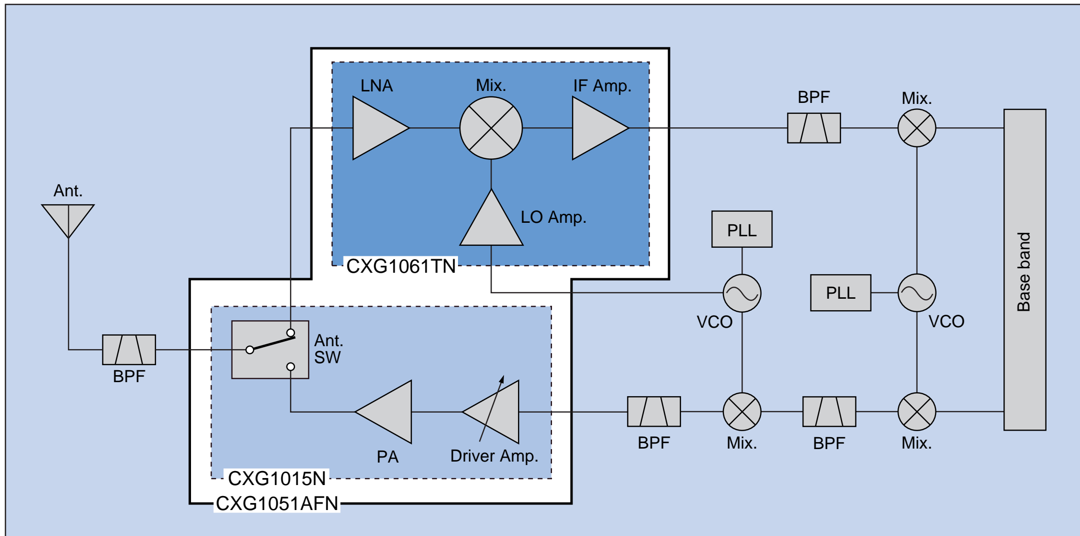
Reduced Current Drain in both the Power Amplifier/Switch and Low-Noise Amplifier/Mixer Blocks

In the power amplifier/switch block, the combination of revisions to sections of the matching circuit with the reduced thermal resistance and ideal ground described above allows this device to achieve a current drain of 150 mA, which is 10 mA lower than the 160 mA current drain of conventional type products. (See figure 3.) Additionally, while still providing fully adequate sensitivity characteristics in the low-noise amplifier/mixer block, the current drain in this circuit has been reduced from the 7 mA of the conventional type to 5.5 mA in this product. These improvements allow end products to provide longer continuous connect times.

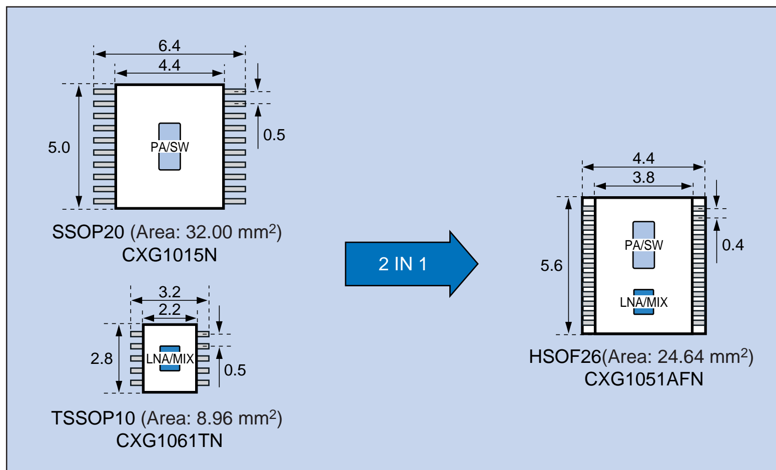
Direct Coupling within the Chip between the Low-Noise Amplifier and Mixer

The most common technique in the low-noise amplifier/mixer block is to separate these two circuits within the chip and use an external filter to exclude unnecessary signals. However, the CXG1051AFN adopts the approach of directly coupling these two components within the IC itself. In this approach the inter-stage matching circuit between the low-noise amplifier and the mixer is given the role of the filter and removes unnecessary signals. Thus no external filter circuit is needed. In the development of this product, we succeeded in improving the image rejection ratio and the 1/2 IF rejection ratio by about 13 dB and about 4 dB. respectively, by optimizing the filter characteristics of the inter-stage matching circuit. (See figure 4.)

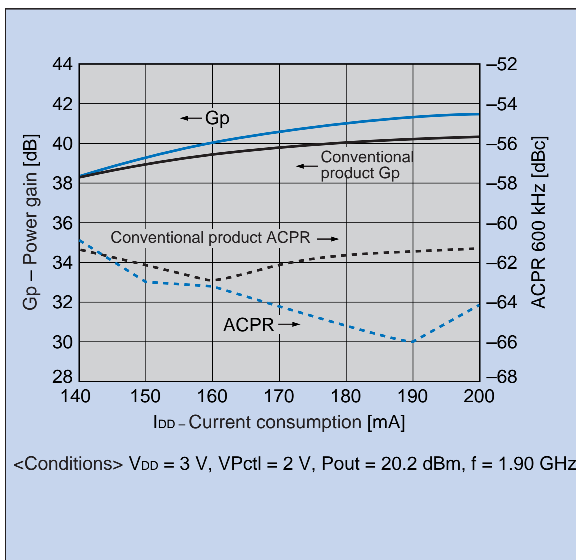




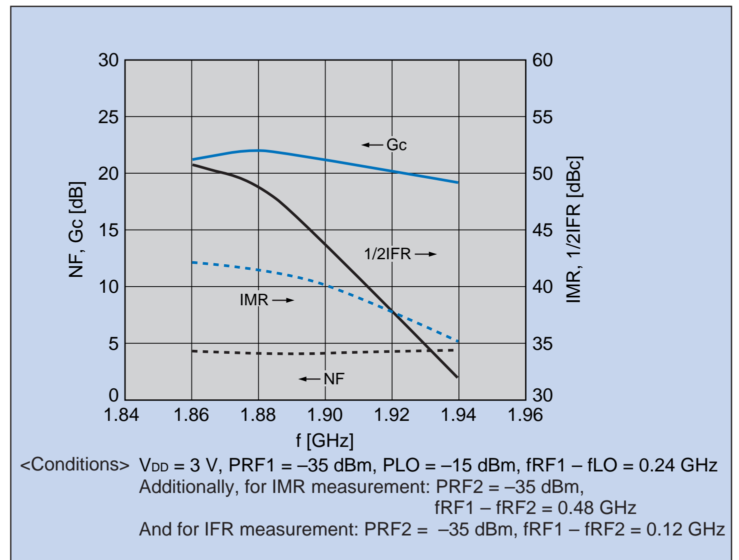
■ **Figure 1 Sample PHS Terminal High-Frequency System Block Diagram**



■ **Figure 2 Comparison of Packages Size with Conventional Products**



■ **Figure 3 PA/SW Transmitter Block Characteristics**



■ **Figure 4 SW Receiver Block and LNA/Mixer Characteristics**