

C5MX Series

C6MX Series

As the anticipated age of the system LSI approaches, Sony has developed two series of embedded gate array products, the C5MX Series and the C6MX Series, which revolutionize conventional technology. These series adopt the latest technology in the basic cells and achieve both the high functionality of standard cells with the short delivery period of gate arrays.

In addition to providing a wide range of function cores and an extensive line of high mounting density packages, these also adopt a scan path based design for test technology.

Thus the C5MX Series and the C6MX Series support the implementation of attractive system LSIs.

- Low power and high integration densities even closer to those of standard cells
- Scan path based design for test technology
- Support for a wide range of function cores
- High mounting density packages (CSP)

■ Low Power and High Integration Densities Even Closer to that of Standard Cells

The C5MX Series adopts an advanced technology called the “NXT structure*1”, which optimizes the basic cell transistor structure to be equivalent to that of standard cell products. As a result the C5MX Series achieves a 24% reduction in power consumption and a 21% improvement in integration density as compared to the conventional C5G Series. (See figure 1.) Thus this series provides performance even closer to that of 0.4- μ m process standard cell products. Additionally, Sony expects to release the C6MX Series as a 0.25- μ m process version of this series in the spring.

*1: NXT structure is a registered trademark of In-Chip Systems, Inc.

■ Scan Path Based Design for Test Technology

These series support the automatic generation of test patterns with a high fault coverage by using a scan path test technology that supports a gated clock, and thus can reduce the number of steps associated with fault detection test pattern generation. This system handles skew during scan in/scan out using dedicated scan path flip-flops. This allows the use of JTAG (IEEE1149.1) for boundary scan testing when the substrate is mounted, and also controls BIST for ROM and RAM testing. A single pin is used as a dedicated test pin.

■ Support for a Wide Range of Function Cores

The C5MX and C6MX Series provide an extensive set of function cores appropriate for implementing system LSIs with complex functionality. These cores not only include analog cells such as converters, but also a wide range of memory cells, multipliers, digital filters, and other high-speed cores with sophisticated functionality. In addition, a set of DRAM cores organized as a library is also provided. Additionally, to support the implementation of attractive system LSIs, a wide range of information processing cores, including a 32-bit RISC CPU, image compression and expansion functions, networking and communication cores, and protocol control cores can also be included. Thus these series make it possible to imple-

ment attractive system LSIs. (See photograph 1.)

■ High Mounting Density Packages (CSP)

Sony supports ultrahigh density FLGA and FBGA (referred to collectively as CSP) multi-pin packages that arrange ball or land type pins in an array on the bottom of the package. These packages can meet needs for multi-pins, lower thermal resistance, and high-density mounting at the same time.

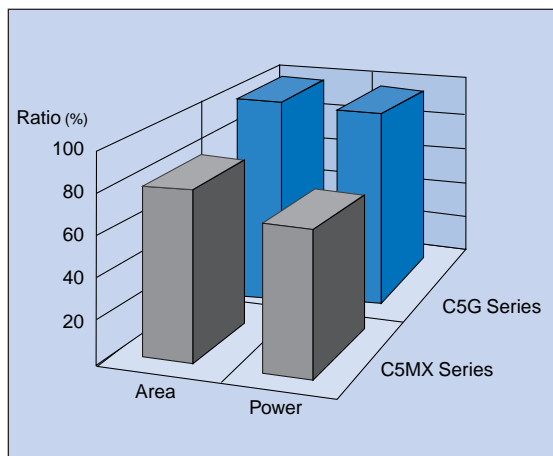
	GFP	FLGA/FBGA
Mounting area (208 pins)	784 mm ²	225 mm ²

V O I C E

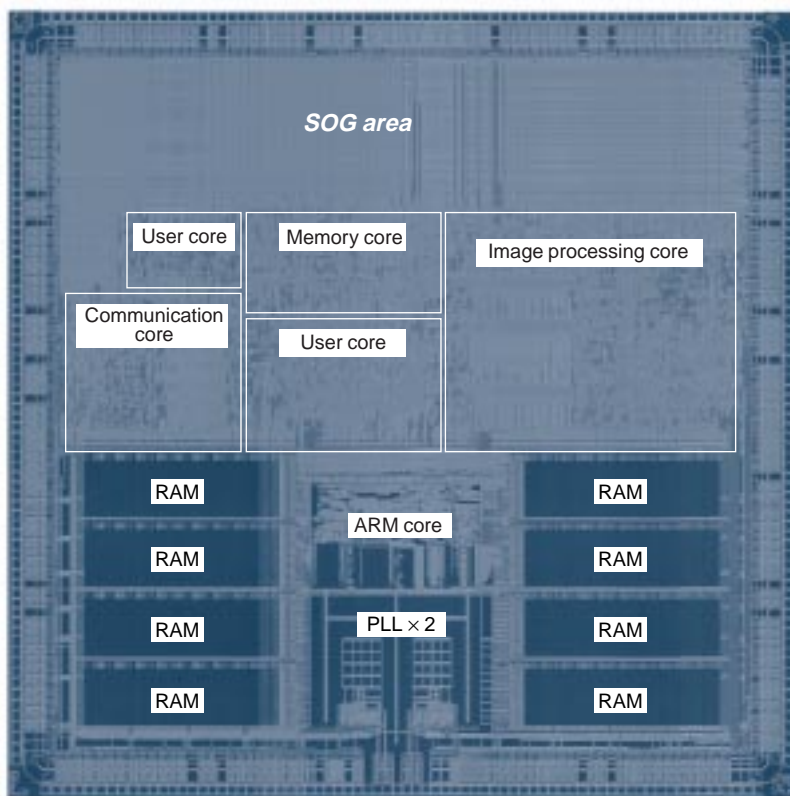
Nowadays one sees the term “system LSI” quite frequently. With the development of the C5MX and C6MX Series products, this term will become even more familiar. These products allow our customers to create LSIs that up to now one would have thought were impossible to implement. Furthermore, they are compact and fast, surprising features for this class of device. You really should try these products.



New Products



■ Figure 1 C5MX/C5G Performance Comparison (For a sample circuit with approximately 50K gates.)



[Chip Spec.]

- Package : 256BGA
- Voltage : 3.3 V
- Process : 0.4 μm (ASC5)
- Frequency : 40 MHz (ARM Core)

[SOG]

- 417K Raw Gates (235K Usable Gates)

[Function Core]

- ARM7TDMI
- SRAM 32 KB
- PLL × 2
- Communication core
- Image processing core

■ Photograph 1 C5MX System LSI Incorporating a High-Performance Core

■ Table 1 C5MX Series Lineup

Product name	C5MX18K	C5MX44K	C5MX55K	C5MX112K	C5MX130K	C5MX190K	C5MX260K	C5MX405K	C5MX618K	C5MX876K
Gate count	18K	44K	55K	112K	130K	190K	260K	405K	618K	876K
Usable gates	11K	26K	33K	67K	78K	114K	153K	231K	340K	464K
Maximum pin count	48	64	80	100	120	144	160	208	256	304
Internal delay time	0.10 ns (2-Input NAND Gate, F/O = 1, L = 0 mm)/0.14 ns (2-Input NAND Gate, F/O = 1, L = standard load)									
I/O levels	LVTTTL, CMOS compatible									
Output drive capability	IoL = 2, 4, 8, 12, 48 (Open Drain) mA									
Supply voltage	3.3 V ± 0.3 V, 2.2 V ± 0.2 V									

■ Table 2 C6MX Series Lineup

Product name	C6MX153K	C6MX207K	C6MX302K	C6MX374K	C6MX457K	C6MX643K	C6MX983K	C6MX1395K	C6MX1971K	C6MX4573K
Gate count	153K	207K	302K	374K	457K	643K	983K	1395K	1971K	4573K
Usable gates	92K	124K	178K	221K	269K	373K	560K	781K	1064K	2268K
Maximum pin count	104	120	144	160	176	208	256	304	360	544
Internal delay time	53 ps (2-Input NAND Gate, F/O = 1, L = 0 mm)/78 ps (2-Input NAND Gate, F/O = 1, L = standard load)									
I/O levels	LVTTTL, CMOS compatible									
Output drive capability	IoL = 2, 4, 8, 12, 48 (Open Drain) mA									
Supply voltage	2.5 V ± 0.2 V, 1.8 V ± 0.15 V									