

Real-Time Video Image Processing in Software

Video DSP

- Allows a wide range of video processing to be implemented in software
- Highly parallel processing provides 4.3 GOPS of arithmetic processing
- Architecture appropriate for converting between image display formats

The Sony DSP introduced here includes two SIMD*1 highly parallel linear array structured processor sets which consist of 1080 individual processor elements and was designed for video applications that require enormous arithmetic processing capabilities on the order of the 4.3 GOPS*2 provided by this device. This DSP supports flexible processing of high-speed real-time video data in TV and personal computer application, in particular, allowing a wide range of signal-processing functions and conversion operations between transmission methods (composite/component) and between display formats (e.g. 1080i, XGA) to be implemented in software.

ASIC and DSP

While there are already a wide variety of digital video related electronic products in the marketplace, the majority of these are implemented using ICs that have structures that are specific to the application, in other words, ASICs. These are referred to as “hard-wired structures.” That is, the most common implementation technique in the audio area, which involves implementing the actual application with a program running on a general-purpose DSP or similar chip is almost never used in the video area.

*1 SIMD: Single instruction stream/multiple data stream

*2 GOPS: Giga operations per second

TV

- Format conversion
 - I/P* conversion
 - Zooming effects
 - Noise reduction
 - Image enhancement
 - Color space conversion
- * Interlace/Progressive



Video DSP



Computer Displays (LCD and other displays)

- Arbitrary pixel size conversion
- I/P conversion
- Gamma correction (simplified processing)
- Multiformat monitors (including SVGA, XGA, NTSC, HDTV, and others)

Digital Cameras

- Camera signal processing
- Gamma correction (simplified processing)
- NTSC encoding



This DSP supports arbitrary conversion between a wide variety of video signal formats and a wide range of video signal processing.

■ Figure 1 Video DSP Applications

Software Processing of Video Signals

This is due to the difference in the bandwidths of video and audio signals, and results directly from the fact that video data rates are three orders of magnitude higher than those required for audio processing. For example, a normal NTSC TV signal has a bandwidth of about 4 MHz, and a sampling rate of 13.5 or 14.318 MHz is normally selected. For a program to process this data, it would have to execute several instructions to complete the stipulated processing of each data point in the extremely short interval of about 70 ns before the next data arrives. For a normal DSP that only has a single data path and arithmetic unit, this would require an operating speed in the GHz or higher range, which is extremely difficult to achieve with current technology. (See table 1.)

Linear Array Structure

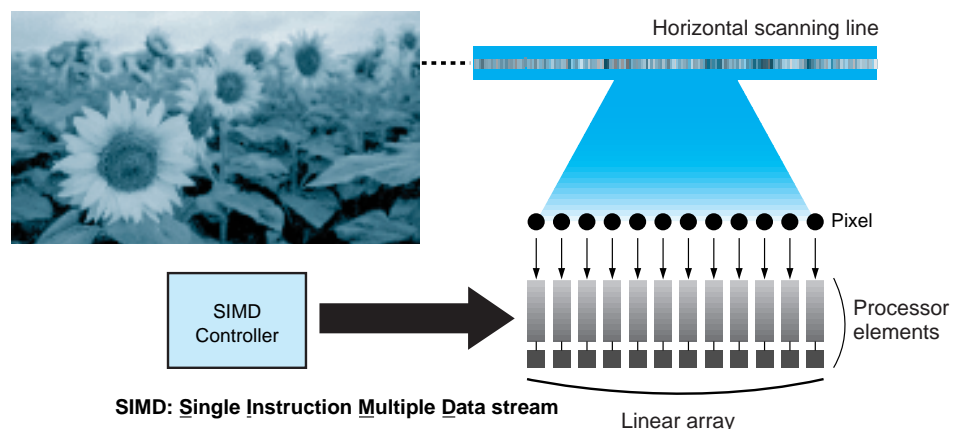
While there have been impressive advances in semiconductor technology, a parallel processing structure of some sort will remain, for the near future at least, indispensable for processing video signals in real time in software. Thus an arithmetic block with multiple data paths is required.

While there are several parallel processor architectures, each has its own advantages and disadvantages. The video DSP described here adopts a linear array structure (see figure 2) that is most appropriate for TV video signal processing and for conversion between various video formats including personal computer video outputs.

The linear array structure arranges a large number of parallel processor elements in a one-dimensional array. In video applications, processor elements are allocated to pixels on the horizontal scanning line in a one-to-one relationship.

■ **Table 1** Bandwidths and Sampling Frequencies used for Real-Time Signal Processing

	Bandwidth	Sampling frequency
Voice	3kHz	8kHz
Audio	20kHz	44.1kHz, 48.0kHz, etc.
TV telephone	Up to 1MHz	3.1MHz
Standard TV	4 to 5MHz	14.318MHz, 13.50MHz, etc.
HDTV	20 to 30MHz	74.25MHz, 48.00MHz, etc.



■ **Figure 2** Linear Array Structure

SIMD Program Control

This DSP adopts the SIMD technique as its basic program control strategy. This refers to the technique of using parallel processors with multiple data paths and arithmetic units and linking them together under the control of a single program control unit. Note that the term MIMD*3 refers to systems in which each of the parallel data path and arithmetic units has its own independent program control unit.

When a video DSP that has the structure shown in figure 2 processes, for example, a normal NTSC TV signal, which has a horizontal scan period of about 63.6 μ s, the program processing period (or cycle) will be that of the input signal. This means that if the DSP has a clock frequency of 50 MHz, then it will be able to perform over 3000 instruction execution cycles per horizontal scan period in real time.

Although SIMD control is a simple structure and special techniques are required to perform separate operations in the individual unit processors, most of the processing in image processing applications, which require enormous amounts of iterated calculations, can be performed without problem by SIMD control. In particular, the SIMD control technique can be said to be optimal for

consumer applications, since it allows the implementation of parallel processors with excellent price performance characteristics.

*3 MIMD: Multiple instruction stream, multiple data stream

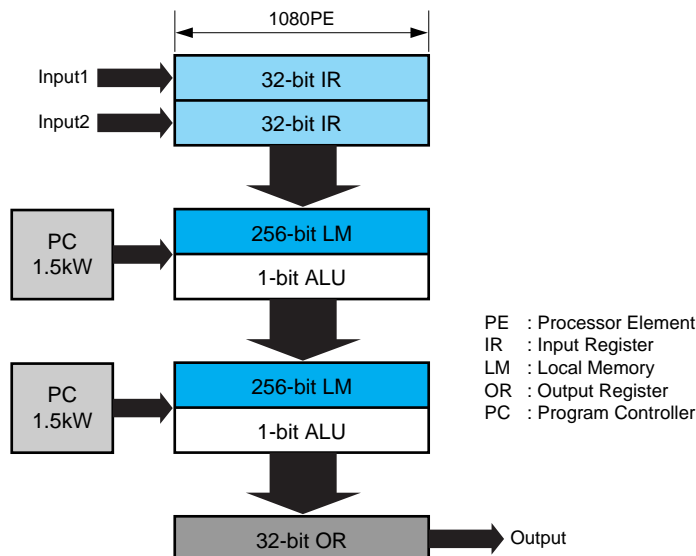
Architectural Overview

Figure 3 presents an overview of the architecture of this DSP. The Sony video DSP consists of two linear array architecture processor sets connected in series. Each processor set uses the SIMD control technique for program control and an MIMD control technique is adopted overall for the two processor sets. Each processor set handles all of the pixel data for every pixel in a horizontal scanning line at the same time and transfer of data between processors also functions in this manner. This DSP provides memory units before and after the processor sets. There are two input buffer memory units (serial-to-parallel converters) that convert a single scanning line period of 32-bit wide time series video data to parallel, and a single 32-bit wide output buffer memory (parallel-to-serial converter) that performs the reverse operation. Each processor set consists

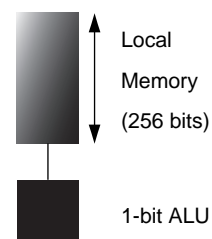
of 1080 processors, a number adequate not just for standard TV signals, but also for video signals that conform to the VGA, SVGA, and XGA VESA standards. That is, the input buffer memory, the two processor sets, and the output buffer memory implement an extremely wide bass bandwidth.

Processor Elements

The Sony video DSP processor elements are 1-bit processors that consist of a 1-bit arithmetic unit and 256 bits of memory as shown in figure 4. While the 1-bit arithmetic units include circuits such as registers and selectors, they consists of a full-adder ALU and the logic circuits required for multiplication based on the second-order Booth algorithm, and as such are extremely simple devices. Three-port memories are used as the 256-bit memory units so that two-argument operations can be executed efficiently.



■ Figure 3 Structural Overview



■ Figure 4 Processor Element

Program Processing of Video Data

Since the processor elements that correspond to each pixel in the horizontal scanning line are 1-bit processors, programs process one bit of data in each instruction cycle. The parallel data transfers between the input buffer memories, the two processor sets, and the output buffer memory are also performed 1 bit at a time. That is, the 3000 instructions mentioned earlier referred to bit instruction units. Although programming at this low level may seem inconvenient, it actually turns out to be a highly efficient programming technique in which no arithmetic unit cycles are wasted. Furthermore, many operations can be written as word instructions and expanded to bit instructions by the macro assembler.

TV Video Signal Processing Applications

A wide range of video signal-processing functions for TV video signals can be implemented and freely combined by programs for this Sony DSP. These functions include filter processing such as bandwidth limiting, noise exclusion, and compensation calculations, and image synthesis operations such as color matrix processing and chroma key processing. High-resolution video signals that require more than the 1080 pixels and thus more than 1080 processor elements can be handled easily by connecting multiple chips due to the excellent expandability of this design.

Display Format Conversion Applications

To handle a wide variety of display formats, such as DTV, and the VGA, SVGA, and XGA formats used by personal computers, applications must be able to freely convert between these

formats. Resolution conversion (i.e. pixel count conversion) is especially indispensable for applications that use displays with fixed numbers of pixels, such as LCD panels. Special efforts have been taken in each of the circuit blocks in this video DSP to assure that it is optimal for resolution conversion.

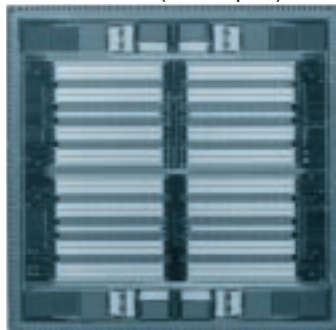
Future Developments

Sony provides a macro assembler based integrated program development environment, and is now developing a macro program library that will provide a wide range of video processing functions. Although the current version of this chip achieves a performance of 4.3 GOPS, which is adequate to provide at least 120 multiply and accumulate operations, Sony will continue to aim for improved performance in future products.

■ Table 2 Main Characteristics

Process	0.4μm CMOS Triple-metal
Number of Transistors	600million
Package	208-pin QFP
Power Supply	3.3V
I/O Data	75MHz 3.3V
Input Data	64bits
Output Data	32bits

Product 1 (developed)



Product 2 (developed)



(Announced at the 1996 ISSCC Conference.)

■ Figure 5 Chip Photographs