

# TTL Input High-Speed 10-Bit 125-MSPS D/A Converter with an Extensive Set of On-Chip Functions

## CXA3197R

The CXA3197R is a bipolar D/A converter that is implemented using a high-speed ECL process.

Sony has already developed ultrahigh-speed 500-MSPS D/A converters, and is now releasing a high-speed D/A converter that achieves low power consumption by taking advantage of those technologies.

- Maximum conversion rates  
PECL operation: 125 MSPS  
TTL operation: 100 MSPS
- Resolution: 10 bits
- Low power consumption: 480 mW
- Data input level: TTL
- Clock and reset signal input levels: TTL or PECL
- 2:1 multiplexed inputs
- Clock divide-by-two circuit (with reset function)
- Voltage output (capable of driving a 50-Ω load)
- Single or dual (±) power supply operation
- Reset signal polarity switching function

Earlier D/A converters that provided conversion rates in excess of 100 MSPS required ECL inputs to achieve those rates. However, the CXA3197R high-speed D/A converter includes an on-chip multiplexer function to allow the inputs to be split into two systems, and thus allows direct input of 10-bit data from TTL signals. It achieves a maximum conversion rate of 125 MSPS, and, in addition to the multiplexed operation using a divided-by-two clock, also supports the multiplexed operation in which the clock is divided by two internally using a clock divider circuit that includes a reset pin.

### ■ Extensive Functions

The CXA3197R supports five operation modes so that application designers can select an appropriate mode.

MUX.1A/MUX.1B modes: The internal clock divide-by-two circuit is used and the two input data systems are multiplexed and output as an analog signal. In MUX.1A mode, the clock signal that was divided by two is output from the DIV2OUT pin. This allows the CXA3197R to acquire data synchronized with the DIV2OUT signal by using the DIV2OUT signal to drive the system in the stages prior to the CXA3197R. (See figure 3.) In MUX.1B mode, the DIV2OUT pin remains in the high-impedance state.

MUX.2 mode: The two input data systems are multiplexed using an externally divided-by-two clock and are output as an analog signal.

SELE.A/SELE.B modes: One of the two input data systems is selected and output as an analog signal.

### ■ Interfaces

Data inputs are TTL-level inputs, while the clock and reset inputs can be selected to be either TTL or PECL level inputs. The DIV2OUT signal high level can be controlled to match the input range of the 3-V CMOS system.

### ■ High Slew Rate Analog Output

Since the analog output has a 50-Ω output impedance, it can achieve the high slew rate of 0.85 ns per transition (10 % to 90% at  $V_{fs} = 1$  V). At the same time this output impedance provides reliable matching with transmission systems so that waveforms with minimal reflections can be acquired.

### ■ Surface Mounting Package

The lower power consumption provided by the CXA3197R and the adoption of a low thermal resistance package allow this device to be provided in an ultra-miniature surface mounting 48-pin LQFP package.

### ■ Applications

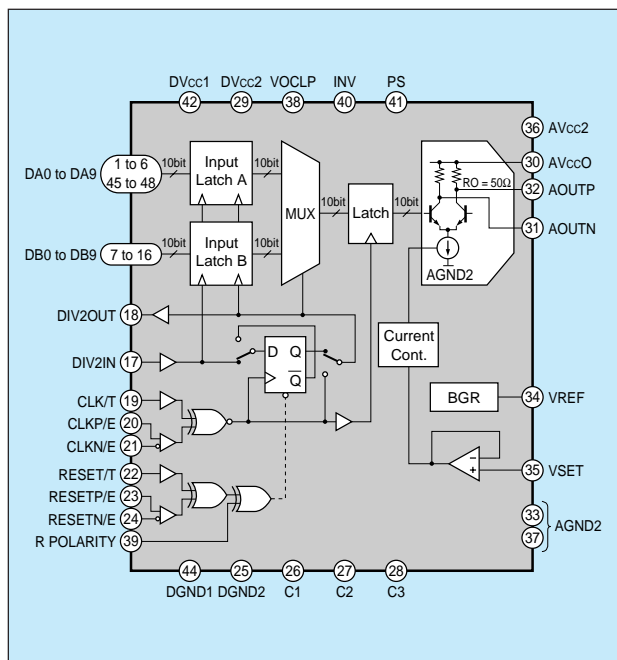
As shown in figure 4, the CXA3197R is optimal for use in applications such as LCD projectors.

## V O I C E

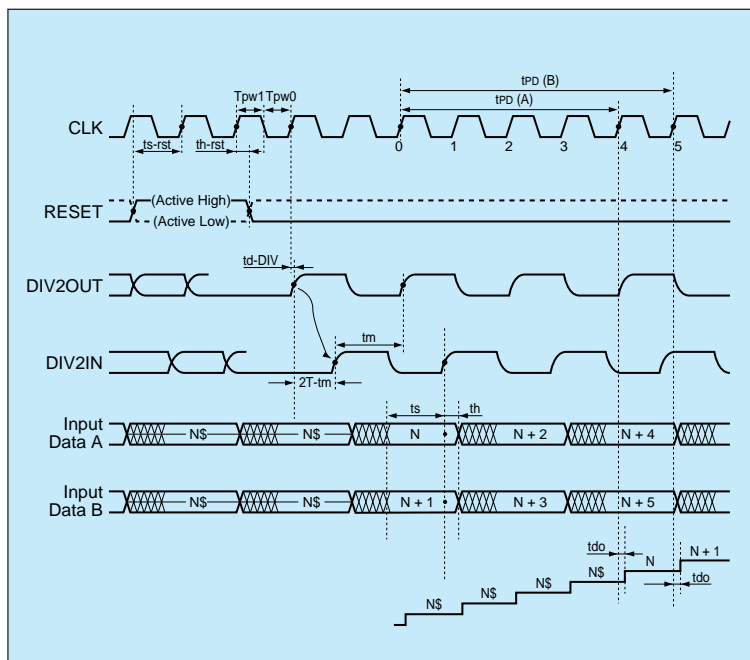
The digital world consists only of zeros and ones. A D/A converter must be used to translate from that world to the analog world. Personally, I find myself somewhat “digital,” at least in my desire to clearly identify things as one or the other, black or white. So I make a point of trying to be more flexible. I hope that my latest design, the CXA3197R, can provide flexibility in your designs.



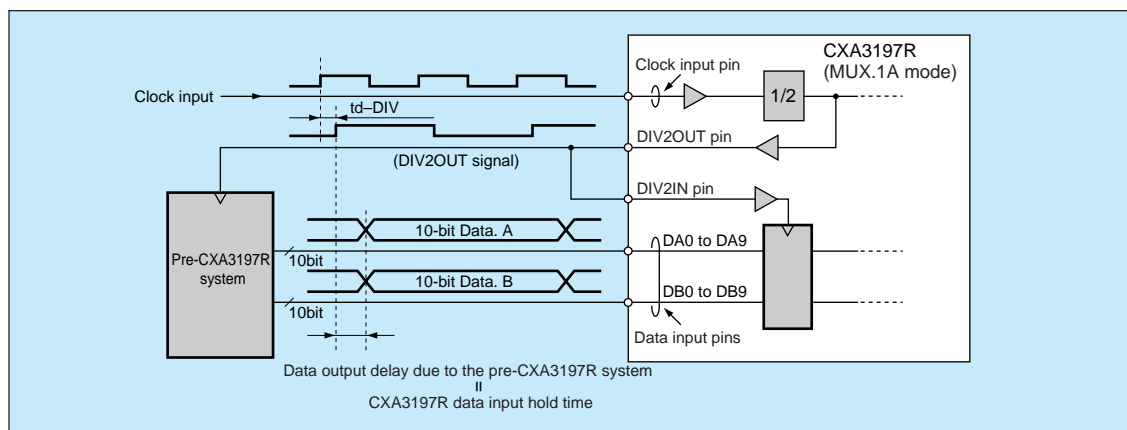
# New Products



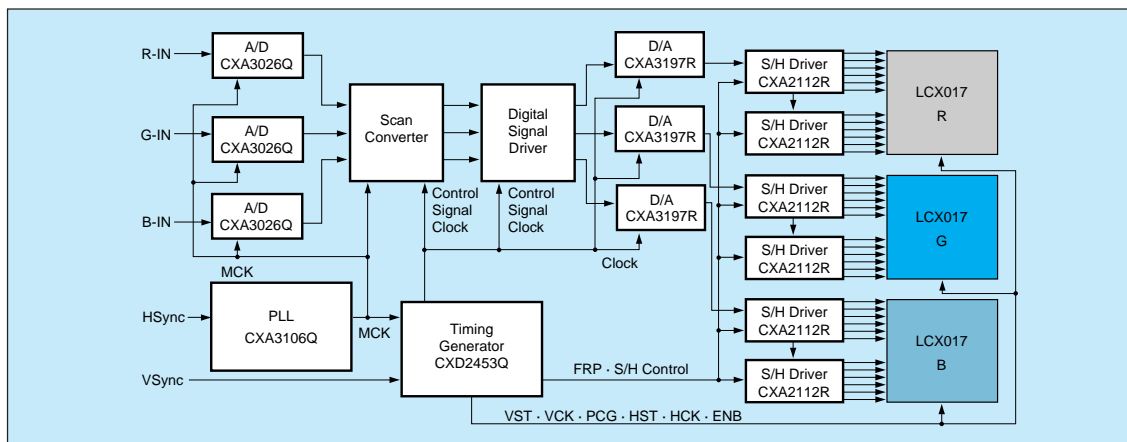
■ Figure 1 CXA3197R Block Diagram



■ Figure 2 Representative Timing Chart (MUX.1A Mode)



■ Figure 3 CXA3197R MUX.1A Mode Operating Example



■ Figure 4 Sample Application: XGA Data Projector