Techno World

Motion Estimation Block and Encoding Controller Integrated on the Same Chip for the First Time in the Industry

Single-Chip MPEG2 Video Encoder LSI

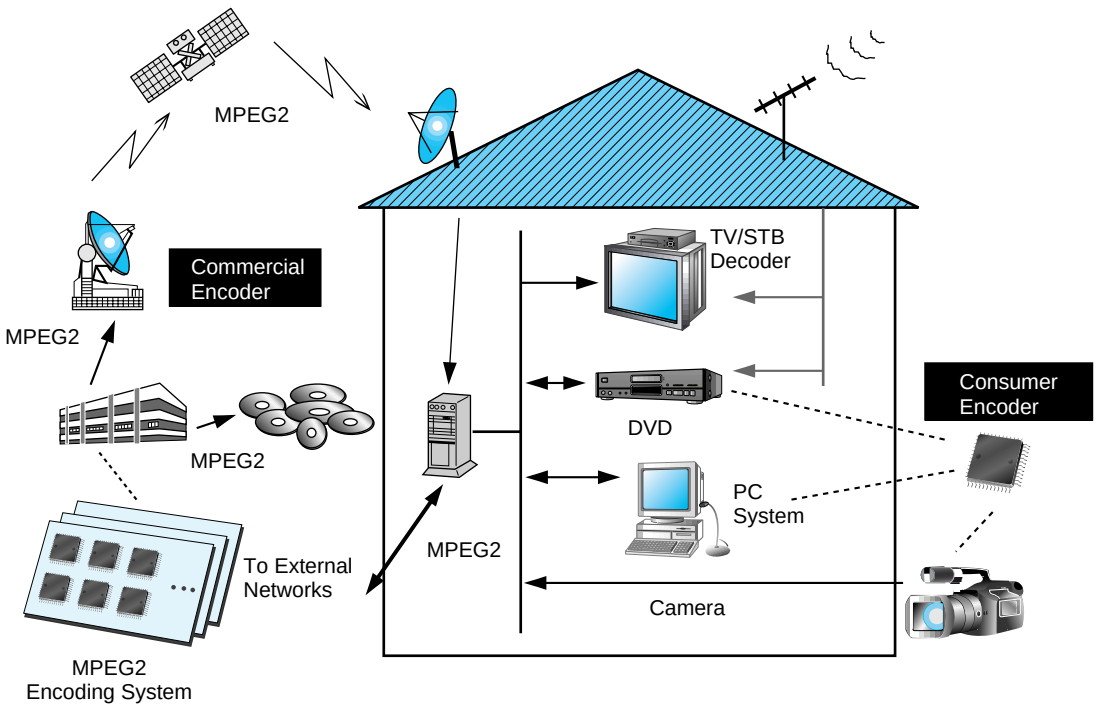
- The industry's widest search range implemented in a single chip
- On-chip motion estimation block and encoding controller
- High integration level and low power consumption achieved
- MPEG2 MP@ML video encoding for NTSC and PAL achieved

Sony has developed the CXD1922Q MPEG2 video encoder LSI designed for optimized MPEG2 MP@ML performance. This LSI concentrates in a single chip the extensive MPEG2 technology that Sony has developed over the last few years. At the same time as achieving the industry's widest search range, the CXD1922Q integrates on a single chip an encoder that includes both the motion estimation block and the encoding controller for the first time in the industry.

Recently, MPEG2 data compression has come to be widely used in areas such as DVD recording and digital broadcasting to record and transmit with high quality the large volumes of image data associated with these applications. The compression of moving images according to the MPEG2 standard and the motion estimation required for that compression require large amounts of arithmetic operation and complex control. Since this processing has been implemented with multiple LSIs previously, end products had large circuits and high power consumption. This has made it difficult to develop consumer applications.

The MPEG2 video encoder LSI we have now developed uses an adaptive motion estimation algorithm designed to be optimal for the MPEG2 standard. This algorithm not only reduces the vast amount of arithmetic operation required for moving image compression, but at the same time also achieves the widest search range (-288 to +287.5 pixels in the horizontal direction and -96 to +95.5 pixels in the vertical direction) available in the electronics industry. This allows the recording and transmission, with minimal image quality degradation, of images with rapid motion, such as sports scenes, and images in which the video camera was moved rapidly either horizontally or vertically.

By fabricating the CXD1922Q in a 0.4-µm CMOS process and by using optimized designs, such as the adoption of



■ Figure 1 Development Background

a multi-clock system incorporating a built-in PLL circuit, Sony was able to create an encoder that includes both the motion estimation block and the encoding controller in a single chip. In addition to achieving the high density of about 4.5 million transistors integrated on a 13.7 × 12.4 mm chip, the CXD1922Q also achieves the low power consumption of 1.2 W.

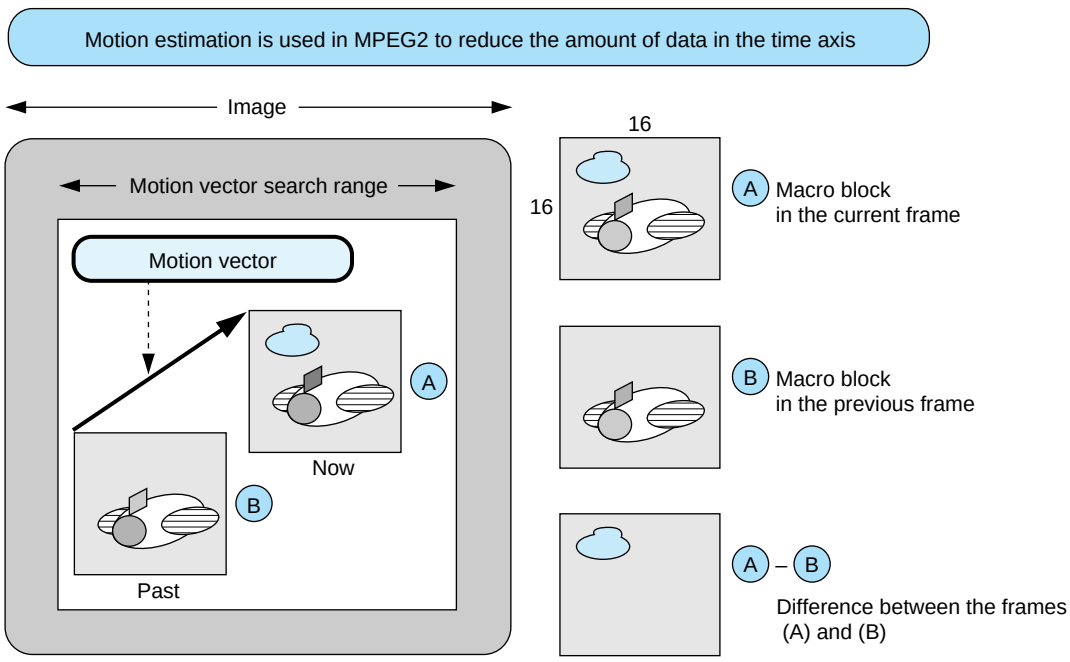
Here we would like to introduce the main features of the electronics industry's most advanced MPEG2 video encoder LSI, as well as present our future development plans in this area.

Achievement of the Industry's Widest Search Range in a Single Chip

The majority of the arithmetic operation required for MPEG2 compression is used for motion estimation. In particular, it would require 108 chips using Sony's previous LSIs to achieve the search range provided by the CXD1922Q. An adaptive motion estimation algorithm optimized for the MPEG2 standard is adopted in the Sony CXD1922Q MPEG2 video encoder LSI just developed. The use of this algorithm suppresses increases in power consumption and increases in the number of chips required to expand the search range and allowed us to implement this functionality in a single chip. The search range achieved by the CXD1922Q covers -288 to +287.5 pixels in the horizontal direction and -96 to +95.5 pixels in the vertical direction. This corresponds to twice the range in the vertical direction and three times the range in the horizontal direction of earlier Sony products, and is the widest range of any product in the industry. Figure 2 shows the concepts behind motion estimation technology. Expanding the search range allows images with rapid motion, such as sports scenes, and images in which the video camera was moved rapidly to be handled with minimal image degradation.

Incorporation of a Newly-Developed Encoding Controller

The recording and transmission of compressed image data using MPEG2 requires large amounts of arithmetic operation and complex control. Since this arithmetic operation and control was previously implemented with multiple chips, applications had large circuits and high power consumption. Thus the common sense in the electronics industry has been that MPEG2 is not practical for consumer products. However, the CXD1922Q MPEG2 video encoder LSI just developed implements, in a single chip, an encoder that includes both the motion estimation block and encoding control. This means that in addition to the complex motion estimation control and bit rate control, timing control for the whole LSI and memory management can be handled completely by internal LSI processing.



■ Figure 2 Motion Estimation Technology

High Integration and Low Power Consumption Achieved

Table 1 lists the main specifications of this MPEG2 video encoder LSI, and table 2 presents a comparison with products of other electronics manufacturers. The main features of this device are the implementation of the functionality in a single chip by the use of high integration level technology, and a significant reduction in power consumption.

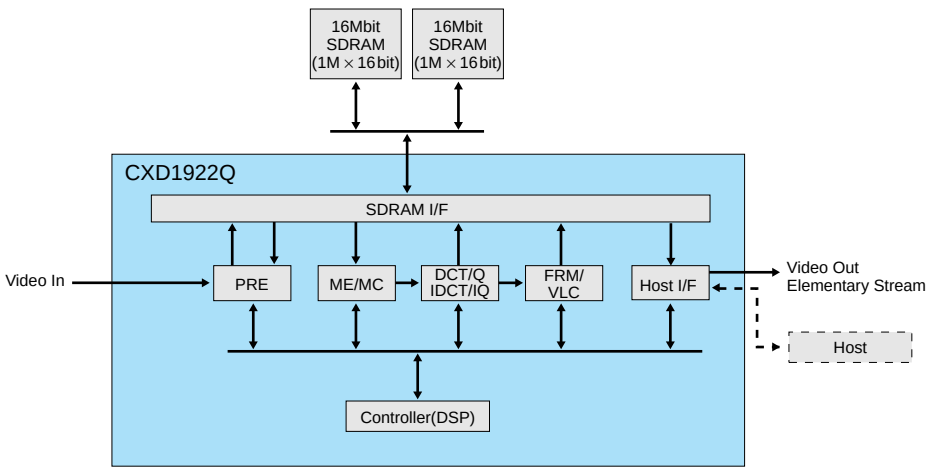
Earlier LSIs required between 3 and 10 LSIs for this functionality, and when the peripheral units are included, total systems required several printed circuit boards each about letter paper size. Now, we at Sony have integrated this functionality on a single chip. This required first the development of an architecture appropriate for a highly integrated system and reduced power consumption, and then the achievement of increased device density to allow 4.5 million transistors to be integrated on a single 13.7 × 12.4 mm chip using a 0.4-µm CMOS process. Finally, the adoption of a multi-clock system*[1] that generates clock signals according to the required operating speed using an on-chip PLL circuit and distributes those clock signals to each block allowed us to suppress power dissipation to 1.2 W, which is about 1/10 that of previous implementations.

Note

*[1] Multi-clock system: The CXD1922Q uses a 67.5-MHz clock for SRAM control, which requires high-speed control, a 45-MHz clock for the motion estimation and motion compensation blocks which have a large arithmetic operation load, a 22.5-MHz clock for the variable length encoding block and local decoding block, which have comparatively lower processing requirements, a 13.5-MHz clock for the front-end filters, and a 27-MHz clock for the DSP core.

■ Table 1 Main Specifications of the CXD1922Q MPEG2 Video Encoder

Functions	MPEG2 MP@ML real-time video encoder NTSC : 720 × 480 at 30 fps (M ≤ 3) PAL : 720 × 576 at 25 fps (M ≤ 3)
Search range	Horizontal : -288 to +287.5 pixels Vertical : -96 to +95.5 pixels
Motion detection technique	Adaptive motion detection algorithm
External memory	32Mbits (16Mbits × 2)
Semiconductor fabrication process	0.4-µm three-layer metal CMOS process
Supply voltage	Single 3.3-V power supply
Clock frequency	External clock input operation : 27 MHz Internal operation : 67.5, 45, 27, 22.5, and 13.5 MHz
Power consumption	1.2W
Number of transistors	About 4.5 million
Package	208pin QFP
Chip size	13.7mm × 12.4mm



■ Figure 3 CXD1922Q Block Diagram

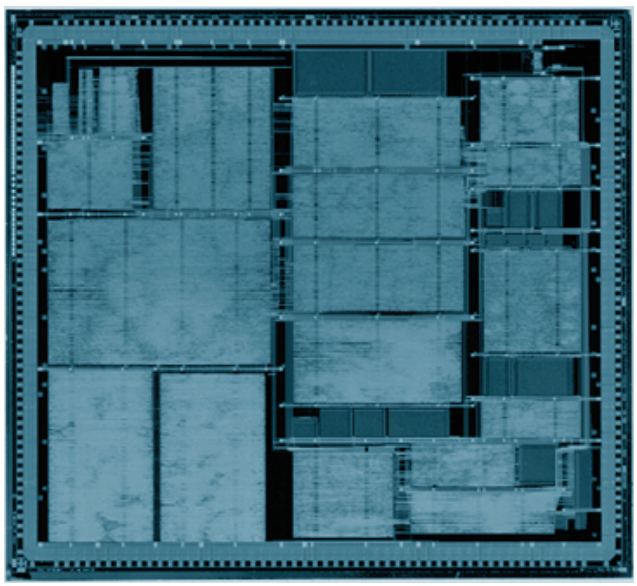
Achievement of an MPEG2 MP@ML Video Encoder for NTSC and PAL

The CXD1922Q encodes either NTSC or PAL video signals with 32 Mbits of external memory, the smallest amount required by any current product. Additionally, the CXD1922Q supports both NTSC and PAL at up to M= 3. The input block supports the 4:2:2 format of the ITU-R Rec.601 standard, and after internally converting the input data to the 4:2:0 format which is specified by the MPEG2 Main Profile, it outputs an MPEG2 video elementary stream.

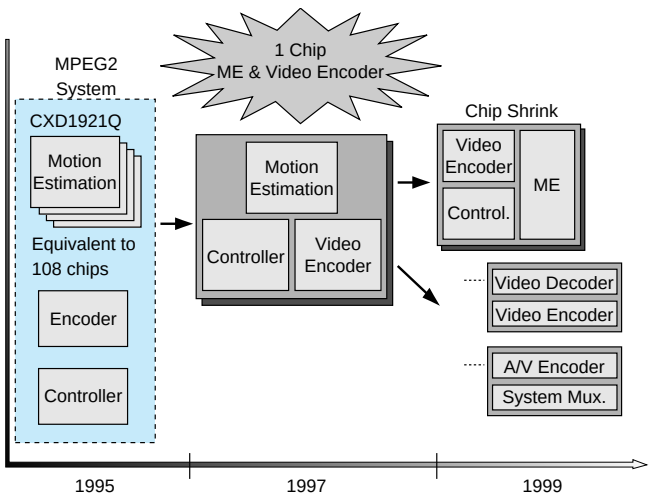
Future Developments

The competition in development related to digital TV, which will come online in a few years, is already fierce in Europe, the USA, and Japan. The MPEG2 video encoder LSI introduced here achieves MPEG2 compression of moving image data with higher quality and with a smaller scale circuit than earlier products. Since it also features significantly reduced power consumption, we are confident that the application areas for this LSI will expand to include consumer products. Towards this end we are investigating the possibilities of implementing audio encoder, system multiplexers, and video decoders as single chips, to achieve lower costs, lower power, and higher performance.

Sony is currently proceeding with the development of the CXD1922Q MPEG2 video encoder LSI, aiming at commercial release by the end of this year.



■ Photograph 1 The CXD1922Q MPEG2 Video Encoder Chip



■ Figure 4 MPEG2 Encoder Development Road Map