

It's Here! After the A/D Converter, Next is a PLL IC
LCD Analog Interface PLL IC

CXA3106Q

The market for LCD monitors and data projectors is growing rapidly. To support the analog input signal processing needs in these products, Sony first released a line of A/D converters, including the CXA3026Q/AQ 8-bit 120/140 MSPS A/D converter and the CXA3086Q 6-bit 140 MSPS A/D converter. Currently, these products enjoy an overwhelming share of the LCD monitor market. Now, we are introducing a PLL IC for use in analog input signal processing.

While engaging in the A/D converter business, we have thoroughly studied the nature of these systems, and have now created an LCD analog interface system with optimal specifications.

- n Sync input frequency: 10 to 100 kHz
- n Clock output signal frequency: 10 to 120 MHz
- n Clock jitter: 1.6 ns p-p (at 75 MHz)
- n Clock delay: 1/16 to 20/16 CLK
- n Sync delay: 1/16 to 20/16 CLK
- n I/O levels: TTL, PECL

Figure 1 shows the analog interface system used by LCD monitors and data projectors. At the left of the figure is a personal computer and at the right is the LCD monitor and data projector. Since the LCD panel requires digital data for each pixel, the LCD monitor and data projector use A/D converters to digitalize the analog R, G, and B signals output by the personal computer. This requires an appropriate clock signal. This clock signal is reproduced from the horizontal synchronizing signal output by the personal computer by the CXA3106Q PLL IC. Figure 2 shows the block diagram of the CXA3106Q, and figure 3 shows the timing chart.

■ PLL Functions Integrated on a Single Chip

The CXA3106Q integrates a phase comparator, a charge pump, a VCO, and a counter on a single chip, and can form a complete system with the addition of just a few external components, such as the resistor and capacitor required for the loop filter. The CXA3106Q also provides a charge pump hold function, an unlock output function, and a 1/2 CLK output function. The CXA3106Q supports not only TTL, but also PECL input and output levels.

■ Resolution

The CXA3106Q sync input frequencies and clock output signal frequencies support analog interface systems from VGA through XGA.

■ Clock Delay Function

The clock output delay can be varied in units of 1/16 of the clock period from 1/16 to 20/16 clocks. Since this delay circuit is built into the PLL loop, there are essentially no sample-to-sample variations or temperature dependency. The A/D converter digitalization for the analog RGB signals from the personal computer can be optimized by adjusting this delay time. The CXA3106Q also provides a delayed sync output in which the sync signal is delayed. Since there is essentially no jitter relative to the clock signal, this signal can be used by system timing circuits.

■ Control

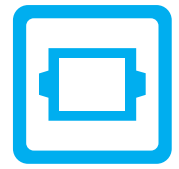
The value of the internal counter (12 bits), the delay value (5 bits), the TTL output on/off state, and the two-stage power saving function can all be set with data sent over a three-wire serial interface.

■ Full Support

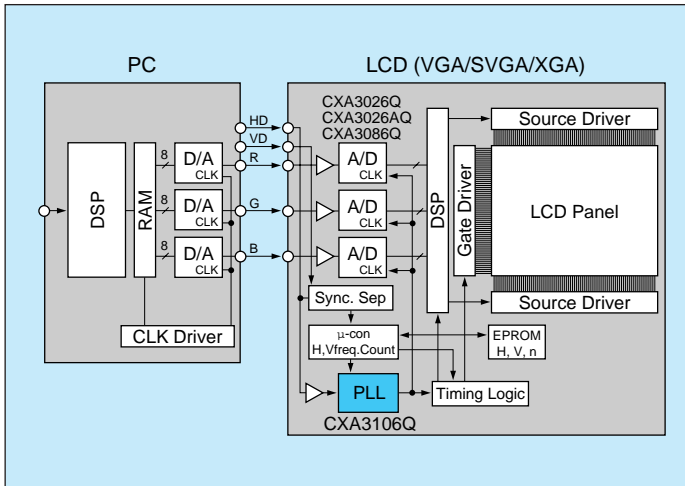
Sony provides an evaluation board, a cable to connect the board to a personal computer printer port, and MS-DOS software (on a floppy disk) for the CXA3106Q so that customers can evaluate the CXA3106Q easily. Sony is also planning to develop additional products in this product line to extend the coverage to the even higher resolution of SXGA systems.

V O I C E

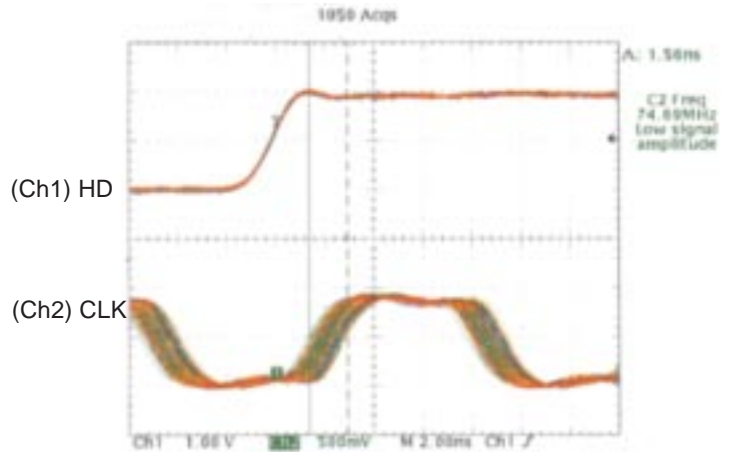
Is it really that difficult to achieve a jitter of less than 1.6 ns? Since the LCD PLL must multiply the horizontal sync signal by 1000 times or more, hopefully, my efforts here will make your work easier.



New Products



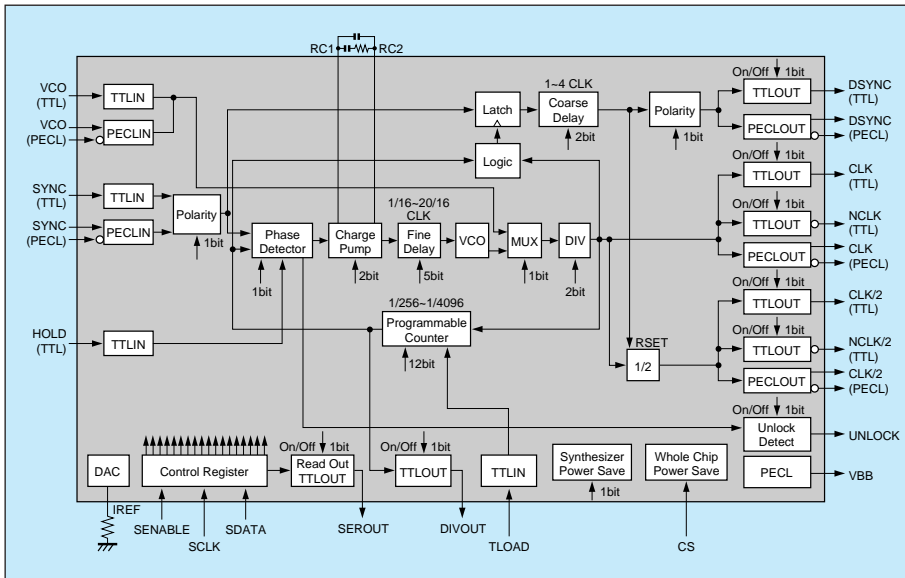
n Figure 1 LCD Analog Interface System Block Diagram



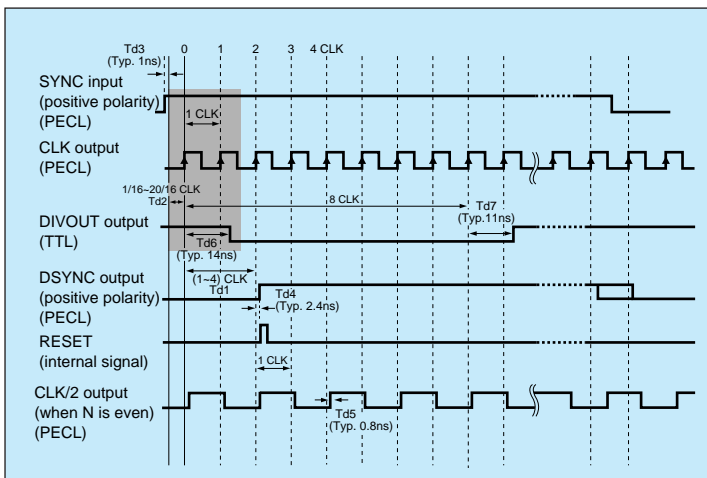
n Figure 4 CXA3106Q Clock Jitter

HD(PC)=56.47kHz
 CLK(PLL)=75.00MHz
 Clock jitter = 1.56 ns p-p
 (the result of integrating 1050 waveforms)

Ch1=1.00V/div
 Ch2=500mV/div
 Timebase=2.00ns/div
 Trigger on Ch1 pos.Edge



n Figure 2 CXA3106Q Block Diagram



n Figure 3 CXA3106Q Timing Chart