

Functions from QPSK Demodulation to Error Correction in a Single Chip Digital Satellite Broadcasting Baseband Signal Processing

CXD1961Q

Satellite broadcasting using digital modulation started in North America in 1994, and will also begin in Japan and Europe this year. In digital satellite broadcasting, a combination of image compression and error correction technologies enables 5 or 6 program channels to be broadcast, with good picture quality, in the bandwidth required for a single conventional analog channel. Providing digital satellite broadcasting receiver functions from digital demodulation to error correction in a single chip, Sony's new CXD1961Q DVB-compliant front-end IC offers high performance at low cost.

- Two high-speed 6-bit A/D converter channels
- Roll-off digital filter
- Clock regeneration circuit supporting multiple symbol rates*1
- Complies with DVB European digital TV standard
- Maximum operating frequency: 60 MHz

*1: Multiple symbol rates: In the DVB standard, the data symbol rate (number of symbols transmitted per second) is not specified, and therefore the clock regeneration frequency must be programmable. With QPSK, one symbol is equivalent to two bits, and the sampling frequency is twice the symbol rate.

■ Digital Satellite Broadcasting

Satellite, CATV, and ground-wave systems have been developed for digital TV using image compression techniques. Satellite systems have made particular progress, and with broadcasts starting this year or in the near future around the world, the era of full-fledged digital satellite broadcasting is fast approaching. Sony's new CXD1961Q IC, incorporating the so-called front-end functions of digital demodulation through error correction in a single chip, should make a significant contribution to the wider use of digital satellite broadcasting.

■ Front-End Compliant with DVB Standard

The DVB (digital video broadcasting) standard for digital TV was formulated by European broadcasters and manufacturers, and is used in Japan and parts of North America as well as in Europe. Satellite broadcasting uses QPSK (quadrature phase-shift keying) as the modulation system and a combination of Reed-Solomon coding and convolutional coding for error correction. The CXD1961Q complies with this DVB standard.

■ Features of the CXD1961Q

A sample reception system is shown in figure 1. The front-end block is positioned directly between the high-frequency signal processing tuner and the MPEG decoder that performs image/audio expansion. Therefore, in this IC section too, the QPSK demodulator is closely linked to the tuner, and in contrast to the large amount of analog signal processing, from the Viterbi decoder that decodes the convolutional codes onward, pure digital signal processing is performed. In developing this new IC, as well as the obvious point of internal IC optimization, consideration was given to providing a simple configuration, including external components and control software. The main features of the CXD1961Q are as follows:

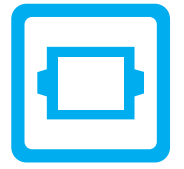
- 1) On-chip high-speed A/D converter, reducing external A/D conversion requirements
- 2) On-chip FIR filter, providing multi-rate support and reducing external LC filter requirements
- 3) Multi-rate oscillator implemented by numerical control oscillator (NCO) and PLL
- 4) AGC (automatic gain control) and AFC (automatic frequency control) circuits
- 5) High-speed, low-power consumption Viterbi decoder

These built-in features mean that the only external components required are a crystal and low-pass filters (for AGC and NCO/PLL), as shown in figure 2. Figure 3 shows the IC block diagram. The CXD1961Q uses a cutting-edge 0.4 μm, 3-layer metal wire CMOS process, and is mounted in a 100-pin plastic QFP package.

V O I C E

With all the talk of new media, the area in which real growth is being achieved is digital satellite broadcasting. While only multichannel TV is offered at the moment, various kinds of data broadcasting are also being studied, and we can expect this new technology to bring significant lifestyle changes in the not too distant future.

- 1) On-chip high-speed A/D converter,



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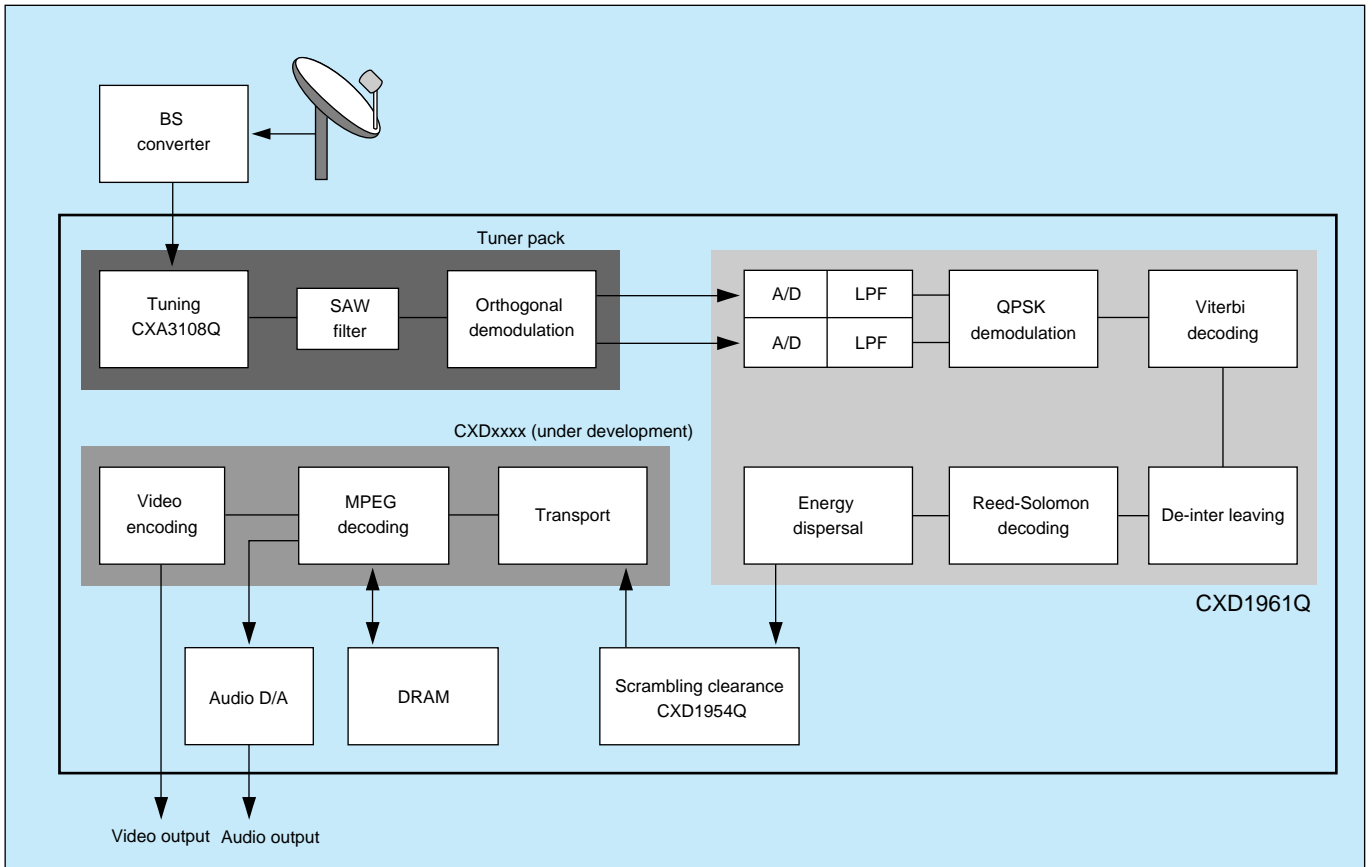


Figure 1 Digital Satellite Broadcasting Set-Top Box Block Diagram

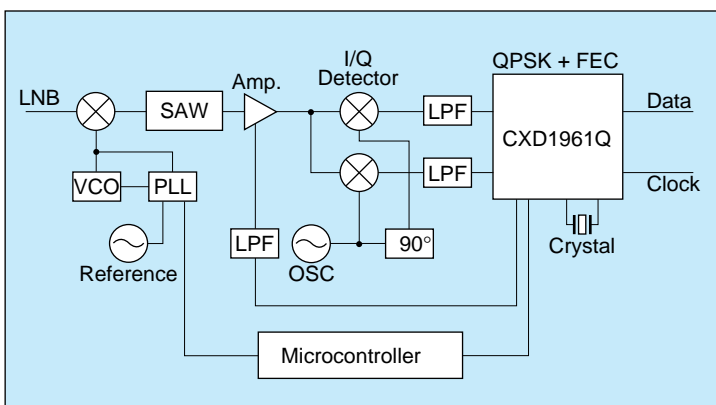


Figure 2 Front-End Block Configuration

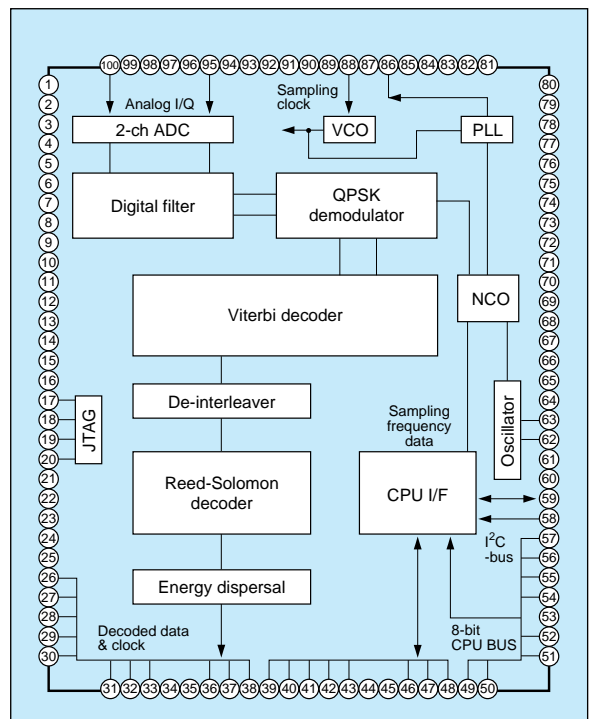


Figure 3 CXD1961Q Block Diagram